VERSACLOCK® LOW POWER CLOCK GENERATOR

IDT5P49EE515

Description

The IDT5P49EE515 is a programmable clock generator intended for low power, battery operated consumer applications. There are four internal PLLs, each individually programmable, allowing for up to five unique non-integer-related frequencies. The frequencies are generated from a single reference clock. The reference clock needs to come from a TCXO sine wave input.

A buffered reference Sine wave output clock is supported with amplitude of 750 mV to 1V, peak to peak.

The IDT5P49EE515 can be programmed through the use of the I^2C interfaces. The programming interface enables the device to be programmed when it is in normal operation or what is commonly known as in system programmable. An internal EEPROM allows the user to save and restore the configuration of the device without having to reprogram it on power-up.

Each of the four PLLs has an 8-bit reference divider and a 11-bit feedback divider. This allows the user to generate four unique non-integer-related frequencies. The PLL loop bandwidth is programmable to allow the user to tailor the PLL response to the application. For instance, the user can tune the PLL parameters to minimize jitter generation or to maximize jitter attenuation. Spread spectrum generation is supported on one of the PLLs.

There are total three 8-bit output dividers. The outputs are connected to the PLLs via the switch matrix. The switch matrix allows the user to route the PLL outputs to any output bank. This feature can be used to simplify and optimize the board layout. In addition, each output's slew rate and enable/disable function can be programmed.

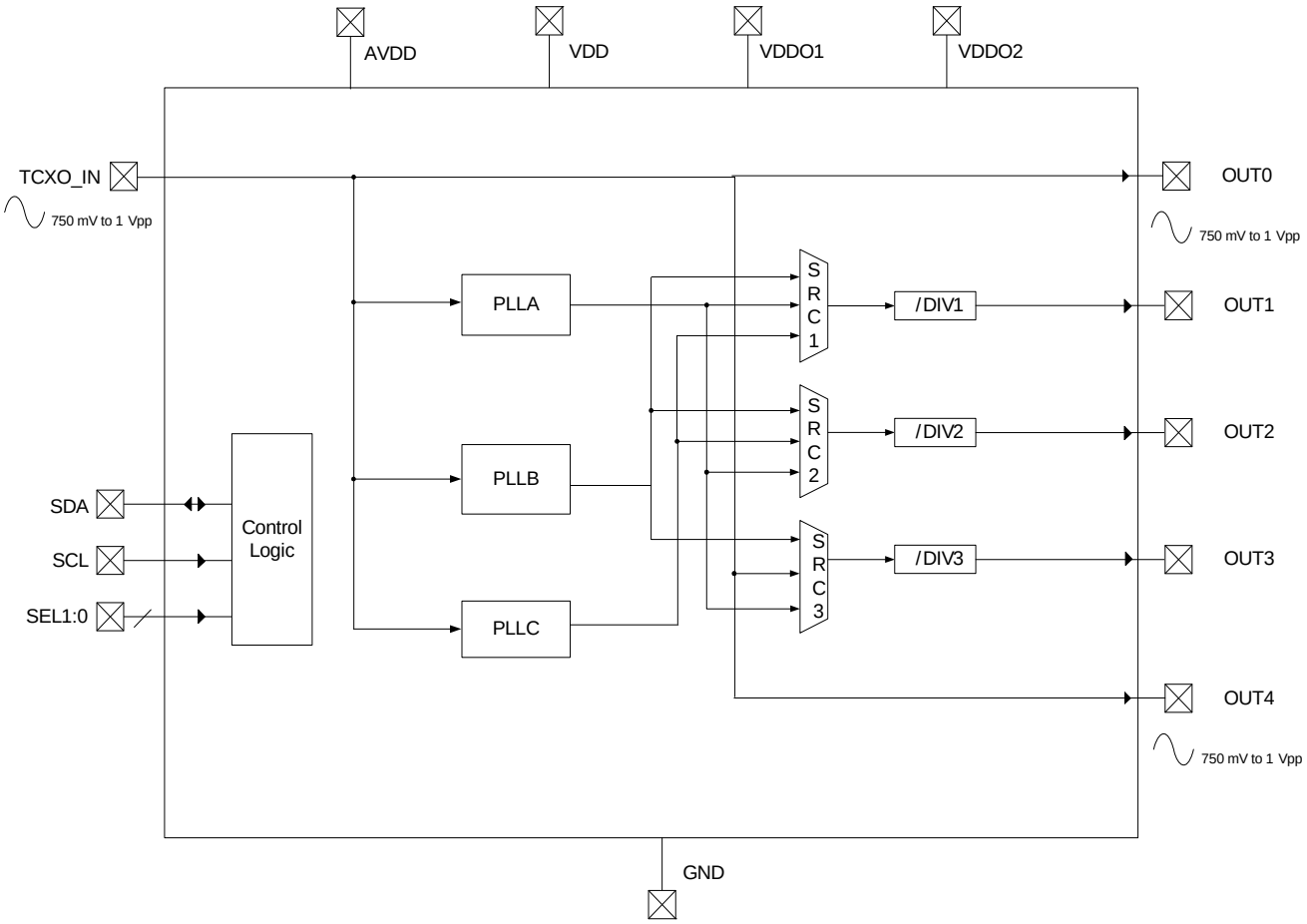
Target Applications

- Smart Mobile Handset
- Personal Navigation Device (PND)
- Camcorder
- DSC
- Portable Game Console
- Personal Media Player

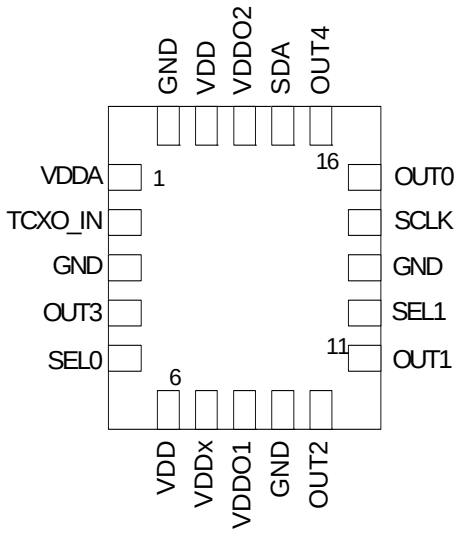
Features

- Four internal PLLs
- Internal non-volatile EEPROM
  - Internal I^2C EEPROM master interface
- FAST (400kHz) mode I^2C serial interfaces
- Input Frequencies
  – TCXO: 10 MHz to 40 MHz
- Two buffered Sine wave output at 750 mV to 1Vpp
- Output Frequency Ranges: kHz to 100 MHz
- Each PLL has an 8-bit reference divider and a 11-bit feedback-divider
- 8-bit output-divider blocks
- I/O Standards:
  – Outputs - 1.8V/2.5V/3.3 V LVTTL/ LVCMOS
- 2 independent adjustable VDDO groups.
- Programmable Slew Rate Control
- Programmable Loop Bandwidth Settings
- Programmable output inversion to reduce bimodal jitter
- Individual output enable/disable
- Power-down/Sleep mode
  – 10µA max in power down mode
- 1.8V VDD Core Voltage
- Available in 20pin 3x3mm QFN packages
- -40 to +85 C Industrial Temp operation

Functional Block Diagram



Pin Assignment



20- pin QFN

Pin Descriptions

Pin Name	Pin #	I/O	Pin Type	Pin Description
VDDA	1	--	Power	Filtered analog power supply. Connect to 1.8V.
TCXO_IN	2	I	Input	TCXO input or external reference clock input.
GND	3		Power	Connect to Ground.
OUT3	4	O	OUTPUT	Configurable clock output 3. Single-ended output voltage levels are register controlled by VDDO1 or VDDO2.
SEL0*	5	I	LVTTL	Configuration select pin. Weak internal pull down resistor.
VDD	6		Power	Device power supply. Connect to 1.8V.
VDDx	7		Power	Device power supply. Connect to 1.8V.
VDDO1	8		Power	Device power supply. Connect to 1.8 to 3.3V. VDDO1 must be the highest voltage on the device. Using register settings, select output voltage levels for OUT1-OUT3.
GND	9		Power	Connect to Ground.
OUT2	10	O	Adjustable	Configurable clock output 2. Single-ended output voltage levels are register controlled by either VDDO1 or VDDO2.
OUT1	11	O	Adjustable	Configurable clock output 1. Single-ended output voltage levels are register controlled by either VDDO1 or VDDO2.
SEL1*	12	I	LVTTL	Configuration select pin. Weak internal pull down resistor.
GND	13		Power	Connect to Ground.
SCLK	14	I	LVTTL	I^2C clock. Logic levels set by VDDO1. 5V tolerant.

OUT0	15	O	Analog Output	Buffered reference Sine wave clock output. Single-ended output voltage levels are controlled by VDDA. Output high-Z when disabled. AC couple wiht 0.1µF capacitor.
OUT4	16	O	Analog Output	Buffered reference Sine wave clock output. Single-ended output voltage levels are controlled by VDDA. Output high-Z when disabled. AC couple wiht 0.1µF capacitor.
SDA	17	I/O	Open Drain	Bidirectional I^2C data. Logic levels set by VDDO1. 5V tolerant.
VDDO2	18		Power	Device power supply. Connect to 1.8 to 3.3V. Using register settings, select output voltage levels for OUT1-OUT3.
VDD	19		Power	Device power supply. Connect to 1.8V.
GND	20		Power	Connect to Ground.
EP	--			Exposed thermal pad should be externally connected to ground.

Note *: SEL pins should be controlled by 1.8V LVTTL logic; 3.3V tolerant.

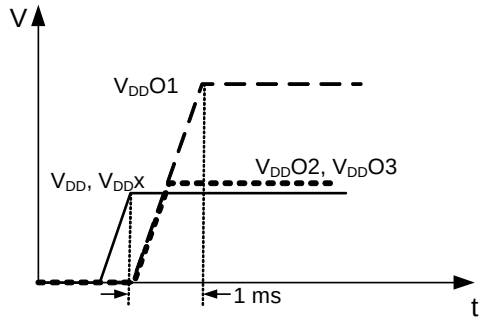
1) Outputs are user programmable to drive single-ended 1.8V/2.5V/3.3V LVTTL as indicated above.

2) Default configuration CLK3=Buffered Reference output. All other outputs are off.

Note 3: Do not power up with SEL[1:0] = 00 (in Power down/Sleep mode).

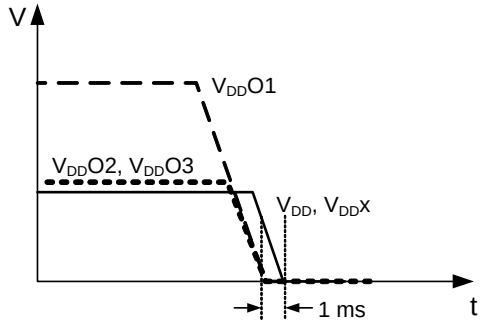
Ideal Power Up Sequence

1) V_{DD} and $V_{DD}x$ must come up first, followed by $V_{DD}O$
2) $V_{DD}O1$ must come up within 1ms after VDD and VDDX come up
3) $V_{DD}O2$ must be equal to, or lower than, $V_{DD}O1$
4) V_{DD} and $V_{DD}x$ have approx. the same ramp rate
5) $V_{DD}O1$ and $V_{DD}O2$ have approx. same ramp rate

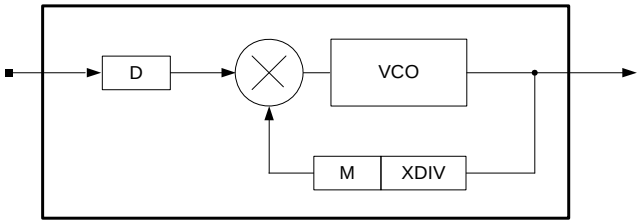


Ideal Power Down Sequence

1) $V_{DD}O$ must drop first, followed by V_{DD} and $V_{DD}x$
2) V_{DD} and $V_{DD}x$ must come down within 1ms after $V_{DD}O1$ comes down
3) $V_{DD}O2$ must be equal to, or lower than, $V_{DD}O1$
4) V_{DD} and $V_{DD}x$ have approx. the same ramp rate
5) $V_{DD}O1$ and $V_{DD}O2$ have approx. same ramp rate



PLL Features and Descriptions



PLL Block Diagram

	Ref-Divider (D) Values	Feedback Pre-Divider (XDIV) Values	Feedback (M) Values	Programmable Loop Bandwidth	Spread Spectrum Generation Capability
PLLA	1 - 255	1 or 4	6 - 2047	Yes	No
PLLB	1 - 255	4	6 - 2047	Yes	Yes
PLLC	1 - 255	1 or 8 bit divide	6 - 2047	Yes	No
PLLD	1 - 255	1 or 4	6 - 2047	Yes	No

Reference Pre-Divider, Reference Divider, Feedback-Divider and Post-Divider

Each PLL incorporates an 8-bit reference-scaler and a 11-bit feedback divider which allows the user to generate four unique non-integer-related frequencies. PLLA and PLLD each have a feedback pre-divider that provides additional multiplication for kHz reference clock applications. Each output divider supports 8-bit post-divider. The following equation governs how the output frequency is calculated.

$$F_{OUT} = \frac{F_{IN} * \left(\frac{XDIV*M}{D}\right)}{ODIV} \quad \text{(Eq. 2)}$$

Where F_{IN} is the reference frequency, XDIV is the feedback pre-divider value, M is the feedback-divider value, D is the reference divider value, ODIV is the total post-divider value, and F_{OUT} is the resulting output frequency. Programming any of the dividers may cause glitches on the outputs.

LOOP FILTER

The loop filter for each PLL can be programmed to optimize the jitter performance. The low-pass frequency response of the PLL is the mechanism that dictates the jitter transfer characteristics. The loop bandwidth can be extracted from the jitter transfer. A narrow loop bandwidth is good for jitter attenuation while a wide loop bandwidth is best for low jitter generation. The specific loop filter components that can be programmed are the resistor via the RZ[4:0] bits, zero capacitor via the CZ[2:0] bits, pole capacitor via the CP[1:0] bits, and the charge pump current via the IP#[2:0] bits.

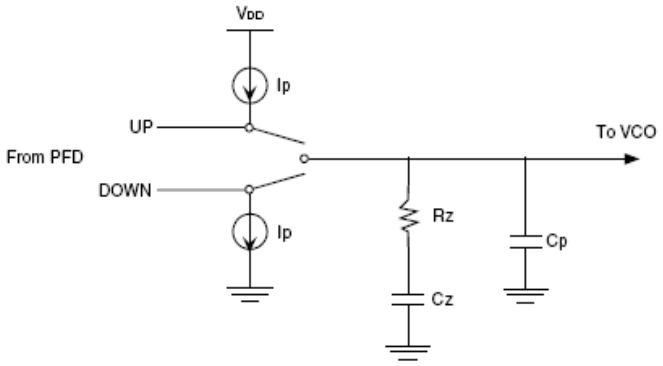
The following equations govern how the loop filter is set:

Zero capacitor (Cz) = 280pF

Pole capacitor (Cp) = 30pF

Charge pump (Ip) = IP#[2:0] uA

VCO gain (K_{VCO}) = 300MHz/V * 2π



PLL Loop Bandwidth:

Charge pump gain ($K\phi$) = Ip / 2π

VCO gain (K_{VCO}) = 350MHz/V * 2π

M = Total multiplier value (See the PRE-SCALERS, FEEDBACK-DIVIDERS, POST-DIVIDERS section for more detail)

$\omega c = (Rz * K\phi * K_{VCO} * Cz)/(M * (Cz + Cp))$

$Fc = \omega c / 2\pi$

Note, the phase/frequency detector frequency (F_{PFD}) is typically seven times the PLL closed-loop bandwidth (Fc) but too high of a ratio will reduce your phase margin thus compromising loop stability.

To determine if the loop is stable, the phase margin (ϕm) would need to be calculated as follows.

Phase Margin:

$\omega z = 1 / (Rz * Cz)$

$\omega p = (Cz + Cp)/(Rz * Cz * Cp)$

$\phi m = (360 / 2\pi) * [\tan^{-1}(\omega c/ \omega z) - \tan^{-1}(\omega c/ \omega p)]$

To ensure stability in the loop, the phase margin is recommended to be > 60° but too high will result in the lock time being excessively long. Certain loop filter parameters would need to be compromised to not only meet a required loop bandwidth but to also maintain loop stability.

Damping Factor:

$\zeta = Rz/2 * (K_{VCO} * Ip * Cz)^{1/2}/M$

Example

Fc = 150KHz is the desired loop bandwidth. The total A*M value is 160. The ζ(damping factor) target should be 0.7, meaning the loop is critically damped. Given Fc and A*M, an optimal loop filter setting needs to be solved for that will meet both the PLL loop bandwidth and maintain loop stability.

Choose a mid-range charge pump from register table

Icp= 11.9uA.

$K\phi * K_{VCO}$ = 350MHz/V * 40uA = 12000A/Vs

$\omega c = 2\pi * Fc = 9.42x10^5\ s^{-1}$

$\omega p = (Cz + Cp)/(Rz * Cz * Cp) = \omega z\ (1 + Cz / Cp)$

Solving for Rz, the best possible value Rz=30kOhms (RZ[1:0]=10) gives

ζ= 1.4 (Ideal range for ζ is 0.7 to 1.4)

Solving back for the PLL loop bandwidth, Fc=149kHz.

The phase margin must be checked for loop stability.

$\phi m = (360 / 2\pi) * [\tan^{-1}(9.42x10^5\ s^{-1} / 1.19x10^5 s^{-1})$
$- \tan^{-1}(9.42x10^5\ s^{-1} / 1.23x10^6\ s^{-1})] = 45°$

The phase margin would be acceptable with a fairly stable loop.

SEL[1:0] Function

The IDT5P49EE515 can support up to three unique configurations. Users may pre-program all configurations, selected using SEL[1:0] pins. Alternatively, users may use I2C interface to configure these registers on- the-fly.

Always power with SEL1=1 and/or SEL0=1.

SEL1	SEL0	Configuration Selections
0	0	Power Down/Sleep Mode
0	1	Select CONFIG0
1	0	Select CONFIG1
1	1	Select CONFIG2

Configuration OUTx IO Standard

Users can configure the individual output IO standard from a single 1.8V power supply. Each output can support 1.8V/ 2.5V or 3.3V LVCMOS. VDDO1 must have the highest voltage of any pin on the device. VDDO2 may have any value between 1.8V and VDDO1.

Programming the Device

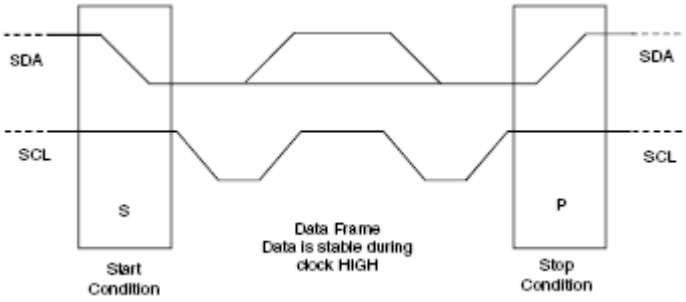
I^2C may be used to program the IDT5P49EE515.

– Device (slave) address = 7'b1101010

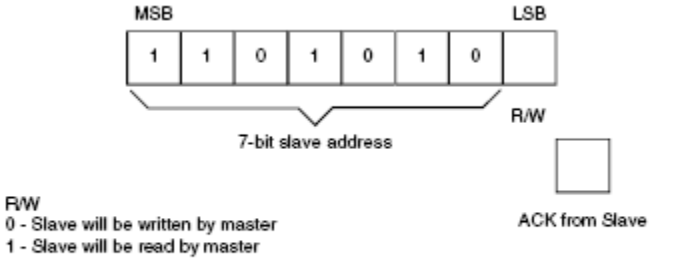
I^2C Programming

The IDT5P49EE515 is programmed through an I^2C-Bus serial interface, and is an I^2C slave device. The read and write transfer formats are supported. The first byte of data after a write frame to the correct slave address is interpreted as the register address; this address auto-increments after each byte written or read.

The frame formats are shown in the following illustration.



Framing



The first byte transmitted by the Master is the Slave Address followed by the R/W bit. The Slave acknowledges by sending a "1" bit.

First Byte Transmitted on I^2C Bus

External I²C Interface Condition

KEY:

From Master to Slave

From Master to Slave, but can be omitted if followed by the correct sequence
Normally data transfer is terminated by a STOP condition generated by the Master. However, if the Master still wishes to communicate on the bus, it can generate a repeated START condition, and address another Slave address without first generating a STOP condition.

From Slave to Master

SYMBOLS:

ACK - Acknowledge (SDA LOW)
NACK - Not Acknowledge (SDA HIGH)
Sr - Repeated Start Condition
S - START Condition
P - STOP Condition

EEPROM Interface

The IDT5P49EE515 can store its configuration in an internal EEPROM. The contents of the device's internal programming registers can be saved to the EEPROM by issuing a save instruction (ProgSave) and can be loaded back to the internal programming registers by issuing a restore instruction (ProgRestore).

To initiate a save or restore using I²C, only two bytes are transferred. The Device Address is issued with the read/write bit set to “0”, followed by the appropriate command code. The save or restore instruction executes after the STOP condition is issued by the Master, during which time the IDT5P49EE515 will not generate Acknowledge bits. The IDT5P49EE515 will acknowledge the instructions after it has completed execution of them. During that time, the I²C bus should be interpreted as busy by all other users of the bus.

On power-up of the IDT5P49EE515, an automatic restore is performed to load the EEPROM contents into the internal programming registers. The IDT5P49EE515 will be ready to accept a programming instruction once it acknowledges its 7-bit I²C address.

Progwrite

S	Address	R/W	ACK	Command Code	ACK	Register	ACK	Data	ACK	P
	7-bits	0	1-bit	8-bits: xxxxxx00	1-bit	8-bits	1-bit	8-bits	1-bit	

Progwrite Command Frame

Writes can continue as long as a Stop condition is not sent and each byte will increment the register address.

Progread

Note: If the expected read command is not from the next higher register to the previous read or write command, then set a known “read” register address prior to a read operation by issuing the following command:

S	Address	R/W	ACK	Command Code	ACK	Register	ACK	P
	7-bits	0	1-bit	8-bits: xxxxxx00	1-bit	8-bits	1-bit	

Prior to Progread Command Set Register Address

The user can ignore the STOP condition above and use a repeated START condition instead, straight after the slave acknowledgement bit (i.e., followed by the Progread command):

S	Address	R/$\overline{W}$	ACK	ID Byte	ACK	Data_1	ACK	Data_2	ACK	Data_last	NACK	P
	7-bits	1	1-bit	8-bits	1-bit	8-bits	1-bit	8-bits	1-bit	8-bits	1-bit	

Progread Command Frame

Progsave

S	Address	R/W	ACK	Command Code	ACK	P
	7-bits	0	1-bit	8-bits:xxxxxx01	1-bit	

Note:
PROGWRITE is for writing to the IDT5P49EE515 registers.
PROGREAD is for reading the IDT5P49EE515 registers.
PROGSAVE is for saving all the contents of the IDT5P49EE515 registers to the EEPROM.
PROGRESTORE is for loading the entire EEPROM contents to the IDT5P49EE515 registers.

Progrestore

S	Address	R/W	ACK	Command Code	ACK	P
	7-bits	0	1-bit	8-bits:xxxxxx10	1-bit	

Note:
During PROGRESTORE, outputs will be turned off to ensure that no improper voltage levels are experienced before initialization.

I²C Bus DC Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	Input HIGH Level		0.7xVDDO1		5.5	V
V_{IL}	Input LOW Level				0.3xVDDO1	V
V_{HYS}	Hysteresis of Inputs		0.05xVDDO1			V
I_{IN}	Input Leakage Current	V_{DD} = 0V			±1.0	µA
V_{OL}	Output LOW Voltage	I_{OL} = 3 mA			0.4	V

I²C Bus AC Characteristics for Standard Mode[1]

Symbol	Parameter	Min	Typ	Max	Unit
F_{SCLK}	Serial Clock Frequency (SCL)	0		100	kHz
t_{BUF}	Bus free time between STOP and START	4.7			µs
$t_{SU:START}$	Setup Time, START	4.7			µs
$t_{HD:START}$	Hold Time, START	4			µs
$t_{SU:DATA}$	Setup Time, data input (SDA)	250			ns
$t_{HD:DATA}$	Hold Time, data input (SDA) [1]	0			µs
t_{OVD}	Output data valid from clock			3.45	µs
C_B	Capacitive Load for Each Bus Line			400	pF
t_R	Rise Time, data and clock (SDA, SCLK)			1000	ns
t_F	Fall Time, data and clock (SDA, SCLK)			300	ns
t_{HIGH}	HIGH Time, clock (SCLK)	4			µs
t_{LOW}	LOW Time, clock (SCLK)	4.7			µs
$t_{SU:STOP}$	Setup Time, STOP	4			µs

1) No activity is allowed on I²C lines until VDD>1.62V.

2) A device must internally provide a hold time of at least 300 ns for the SDA signal (referred to the V_{IH}MIN of the SCLK signal) to bridge the undefined region of the falling edge of SCLK.

I²C Bus AC Characteristics for Fast Mode[1]

Symbol	Parameter	Min	Typ	Max	Unit
F_{SCLK}	Serial Clock Frequency (SCL)	0		400	kHz
t_{BUF}	Bus free time between STOP and START	1.3			µs
$t_{SU:START}$	Setup Time, START	0.6			µs
$t_{HD:START}$	Hold Time, START	0.6			µs
$t_{SU:DATA}$	Setup Time, data input (SDA)	100			ns
$t_{HD:DATA}$	Hold Time, data input (SDA) [1]	0			µs
t_{OVD}	Output data valid from clock			0.9	µs
C_B	Capacitive Load for Each Bus Line			400	pF
t_R	Rise Time, data and clock (SDA, SCL)	$20 + 0.1xC_B$		300	ns
t_F	Fall Time, data and clock (SDA, SCL)	$20 + 0.1xC_B$		300	ns
t_{HIGH}	HIGH Time, clock (SCL)	0.6			µs
t_{LOW}	LOW Time, clock (SCL)	1.3			µs
$t_{SU:STOP}$	Setup Time, STOP	0.6			µs

1) No activity is allowed on I²C lines until VDD>1.62V.

2) A device must internally provide a hold time of at least 300 ns for the SDA signal (referred to the V_{IH}MIN of the SCLK signal) to bridge the undefined region of the falling edge of SCLK.

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the IDT5P49EE515. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Symbol	Description	Max	Unit
V_{DD}	Internal Power Supply Voltage	-0.5 to +4.6	V
V_I	Input Voltage	-0.5 to +4.6	V
V_O	Output Voltage (not to exceed 4.6 V)	-0.5 to V_{DD}+0.5	V
T_J	Junction Temperature	150	°C
T_{STG}	Storage Temperature	-65 to +150	°C

Recommended Operation Conditions

Symbol	Parameter	Min	Typ	Max	Unit
V_{DD} , V_{DD}x	Power supply voltage for VDD	1.71	1.8	1.89	V
V_{DDOX}	Power supply voltage for outputs VDDO1/2/3	1.71	1.8	1.89	V
		2.375	2.5	2.625	V
		3.135	3.3	3.465	V
T_A	Operating temperature, ambient	-40		+85	°C
C_{LOAD_OUT}	Maximum load capacitance (3.3V LVTTL only)			15	pF
C_{LOAD_OUT}	Maximum load capacitance (1.8V or 2.5V LVTTL only)			8	pF
F_{IN}	External reference clock CLKIN	10		40	MHz
t_{PU}	Power up time for all V_{DD}s to reach minimum specified voltage (power ramps must be monotonic)	0.05		5	ms

Capacitance (T_A = +25 °C, f = 1 MHz, V_{IN} = 0V)

Symbol	Parameter	Min	Typ	Max	Unit
C_{IN}	Input Capacitance		3		pF
TCXO Specifications					
TCXO_FREQ	TCXO frequency	10		40	MHz
TCXO_V_{PP}	Voltage swing (peak-to-peak, nominal)	0.75		1.0	V

DC Electrical Characteristics for 3.3 Volt LVTTL [1]

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = 33mA	2.4		VDDO	V
V_{OL}	Output LOW Voltage	I_{OH} = 33mA			0.4	V
I_{OZDD}	Output Leakage Current	3-state outputs			5	µA

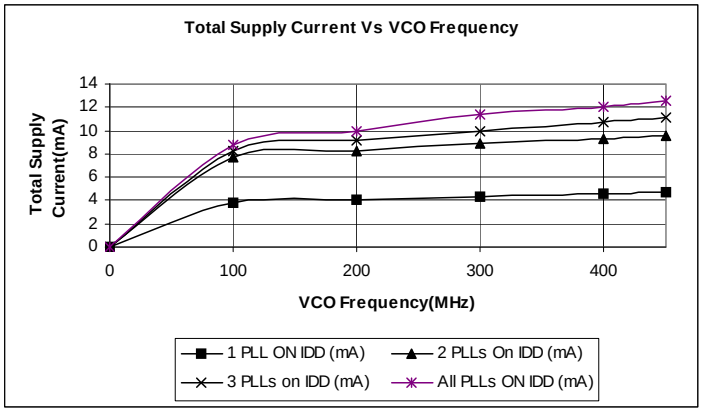
DC Electrical Characteristics for 2.5Volt LVTTL [1]

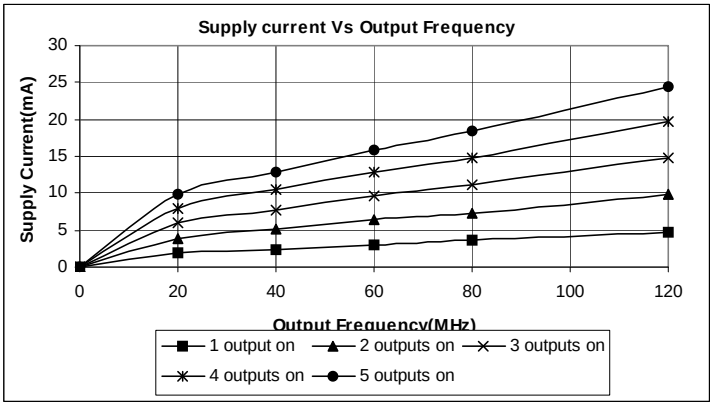
Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = 25mA	2.1		VDDO	V
V_{OL}	Output LOW Voltage	I_{OH} = 25mA			0.4	V
I_{OZDD}	Output Leakage Current	3-state outputs			5	µA

DC Electrical Characteristics for 1.8Volt LVTTL [1]

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{OH}	Output HIGH Voltage	VDD = 1.71V to 1.89V	0.65*VDDO		VDDO	V
V_{OL}	Output LOW Voltage				0.35*VDDO	V
V_{IH}	Input HIGH Voltage	SEL[1:0], 3.3V tolerant	0.75VDD			V
V_{IL}	Input LOW Voltage	SEL[1:0], 3.3V tolerant			0.25VDD	V
I_{OZDD}	Output Leakage Current	3-state outputs			5	µA

Power Supply Characteristics for LVTTL Outputs





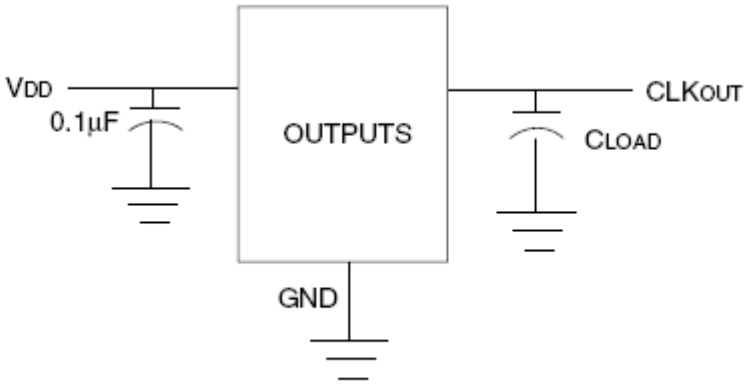
1: See “Recommended Operating Conditions” table. Alway completely power up VDD and VDDx prior to applying VDDO power.

AC Timing Electrical Characteristics

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
f_{IN}	Input Frequency	Input Frequency Limit (TCXO_IN)	10 [1]		40	MHz
1 / t1	Output Frequency	Single Ended Clock output limit (LVTTL) 3.3V	0.001		120	MHz
		Single Ended Clock output limit (LVTTL) 2.5V			110	MHz
		Single Ended Clock output limit (LVTTL) 1.8V			100	MHz
f_{VCO}	VCO Frequency	VCO operating Frequency Range	100		475	MHz
f_{PFD}	PFD Frequency	PFD operating Frequency Range	0.5 [1]		20	MHz
t2	Input Duty Cycle	Duty Cycle for Input	40		60	%
t3	Output Duty Cycle	Measured at VDD/2	45		55	%
t4	Slew Rate, SLEWx(bits) = 00	Single-Ended 3.3V LVCMOS Output clock rise and fall time, 20% to 80% of VDD (Output Load = 7 pF)		5.1		V/ns
	Slew Rate, SLEWx(bits) = 01	Single-Ended 3.3V LVCMOS Output clock rise and fall time, 20% to 80% of VDD (Output Load = 7 pF)		4.4		
	Slew Rate, SLEWx(bits) = 10	Single-Ended 3.3V LVCMOS Output clock rise and fall time, 20% to 80% of VDD (Output Load = 7 pF)		2.8		
	Slew Rate, SLEWx(bits) = 11	Single-Ended 3.3V LVCMOS Output clock rise and fall time, 20% to 80% of VDD (Output Load = 7 pF)		1.8		
t5	Clock Jitter	Peak-to-peak period jitter, CLK outputs measured at VDD/2; f_{PFD} >= 10 MHz Single output frequency only.			100	ps
		Peak-to-peak period jitter, CLK outputs measured at VDD/2; f_{PFD} >= 10 MHz Multiple output frequencies switching.			200	ps
t7	Lock Time	PLL Lock Time from Power-up [1]		5	20	ms
		PLL Lock time from shutdown mode		5	10	ms

1.Time from supply voltage crosses VDD=1.62V to PLLs are locked.

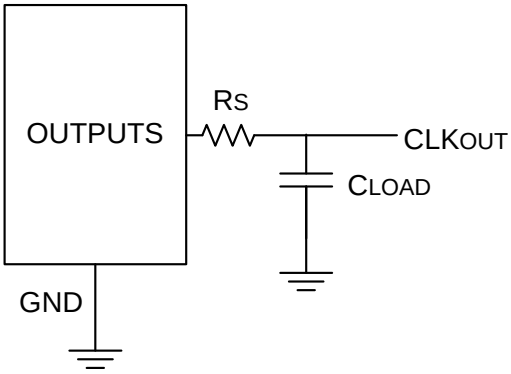
Test Circuits and Conditions [1]



NOTE:
1. All VDD pins must be tied together.

Test Circuits for DC Outputs

Other Termination Scheme (Block Diagram)



LVTTL Output Load: ~7pF for each output

Programming Registers Table

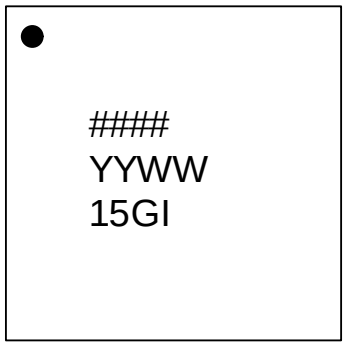
Addr	Default Register Hex Value	Bit # 7	6	5	4	3	2	1	0	Description
0x00	04	Reserved								
0x01	00	Reserved								INV[#] - Invert output# SLEW#[0:1] - output# slew setting 0 0 - 5.1V/ns 0 1 - 4.4V/ns 1 0 - 2.8V/ns 1 1 - 1.8V/ns PS#[2:1] -Power Select 00 - Reserved 01 - CLK# connects to VDDO1 10 - CLK# connects to VDDO2 11 - Reserved
0x02	00	Reserved								
0x03	00	Reserved								
0x04	00	INV[1]	SLEW1[0:1]		Reserved	PS1[2:1]		Reserved		
0x05	00	INV[2]	SLEW2[0:1]		Reserved	PS2[2:1]		Reserved		
0x06	00	INV[3]	SLEW3[0:1]		Reserved	PS3[2:1]		Reserved		
0x07	00	Reserved								
0x08	00	Reserved								
0x09	00	Reserved								
0x0A	00	Reserved								
0x0B	00	Reserved								
0x0C	00	Reserved								
0x0D	00	Reserved								
0x0E	00	REFA[7:0]								**Configuration0** REFA[7:0] - Reference Divide PLLA
0x0F	00	FBA[10:3]								FBA[10:0] - Feedback Divide PLLA
0x10	00	Reserved						FBA[2:0]		
0x11	00	Reserved	XDIVA	RZA[1:0]		IPA[2:0]			Reserved	RZA[1:0] - Zero Resistor PLLA 00 - 5kOhm 01 - 10kOhm 10 - 30kOhm 11 - 80kOhm IPA[2:0] - charge Pump Current PLLA 100 - 6.3uA 101 -11.9 uA 110 - 17.7 uA 111 - 22.7uA
0x12	00	REFB[7:0]								REFB[7:0] - Reference Divide PLLB
0x13	00	FBB[10:3]								FBB[10:0] - Feedback Divide PLLB
0x14	00	Reserved								PLLB Spread Parameters MOD[12:0] NC[10:0] NSS[12:0]
0x15	00	Reserved								
0x16	00	NC[10:3]								
0x17	00	Reserved								
0x18	00	Reserved								
0x19	40	IPB[5:0]						RZB[1:0]		RZB[1:0] - Zero Resistor PLLB 00 - 5kOhm 01 - 10kOhm 10 - 30kOhm 11 - 80kOhm IPB[2:0] - charge Pump Current PLLB 000 - 0.37uA, 100 - 6.3uA 001 - 1.1uA, 101 - 11.9uA 010 - 1.8 uA, 110 - 17.7uA 011 - 3.4uA, 111 - 22.7uA IPB[5:3] - charge Pump Current PLLB 000 - 0.37uA, 100 - 6.3uA 001 - 1.1uA, 101 - 11.9uA 010 - 1.8 uA, 110 - 17.7uA 011 - 3.4uA, 111 - 22.7uA IPB total value = IPB[5:3] = IPB[2:0]
0x1A	00	Reserved							SSENB_B	
0x1B	00	Reserved								
0x1C	00	Reserved								
0x1D	00	Reserved								
0x1E	00	Reserved								
0x1F	00	Reserved								
0x20	00	REFC[7:0]								REFC[7:0] - Reference Divide PLLC
0x21	00	FBC[10:3]								FBC[10:0] - Feedback Divide PLLC
0x22	00	Reserved						FBC[2:0]		

Addr	Default Register Hex Value	Bit # 7	6	5	4	3	2	1	0	Description
0x23	00	XDIVC	RZC[1:0]		IPC[2:0]			Reserved		RZC[1:0] - Zero Resistor PLLC 00 - 5kOhm 01 - 10kOhm 10 - 30kOhm 11 - 80kOhm IPC[2:0] - charge Pump Current PLLC 100 - 6.3uA 101 -11.9 uA 110 - 17.7 uA 111 - 22.7uA
0x24	00	Reserved								
0x25	00	Reserved								
0x26	00	Reserved								
0x27	00	OD1[7:0]								
0x28	00	OD2[7:0]								
0x29	00	OD3[7:0]								
0x2A	00	Reserved								
0x2B	00	Reserved								
0x2C	00	Reserved								
0x2D	00	Reserved						SCR3[1:0]		SRC3[1:0] - OD3 source 00 - off; 10 - PLLA 01 - Reference (square wave); 11 - PLLB
0x2E	00	SCR2[1:0]		SCR1[1:0]		Reserved				SRC1[1:0] - OD1 source 00 - off; 10 - PLLB 01 - PLLA; 11 - PLLC SRC2[1:0] - OD2 source 00 - off; 10 - PLLB 01 - PLLA; 11 - PLLC
0x2F	01	Reserved								
0x30	FF	Reserved								
0x31	00	PDB[4]	Reserved							PDB[4:1] - Powerdown OUT#. PDB#=0, OUT# driven low PDB4 controls OUT0 and OUT4. OE[4:1] - Output enable OUT#. OE#=0, OUT# tri-stated. If PDB#=OE#=0, OUT# driven low
0x32	00	Reserved		OE[3]	OE[2]	OE[1]	Reserved			
0x33	00	Reserved		PDB[3]	PDB[2]	PDB[1]	Reserved			

Addr	Default Register Hex Value	Bit # 7	6	5	4	3	2	1	0	Description
0x34	00	REFA[7:0]								**Configuration1** (See definitions from Configuration0 above)
0x35	00	FBA[10:3]								
0x36	00	Reserved					FBA[2:0]			
0x37	00	Reserved	XDIVA	RZA[1:0]		IPA[2:0]			Reserved	
0x38	00	REFB[7:0]								
0x39	00	FBB[10:3]								
0x3A	00	Reserved								
0x3B	00	Reserved								
0x3C	00	Reserved								
0x3D	00	Reserved								
0x3E	00	Reserved								
0x3F	40	IPB[5:0]						RZB[1:0]		
0x40	00	Reserved						Reserved	SSENB_B	
0x41	00	Reserved								
0x42	00	Reserved								
0x43	00	Reserved								
0x44	00	Reserved								
0x45	00	Reserved								
0x46	00	REFC[7:0]								
0x47	00	FBC[10:3]								
0x48	00	Reserved					FBC[2:0]			
0x49	00	XDIVC	RZC[1:0]		IPC[2:0]			Reserved		
0x4A	00	Reserved								
0x4B	00	Reserved								
0x4C	00	Reserved								
0x4D	00	OD1[7:0]								
0x4E	00	OD2[7:0]								
0x4F	00	OD3[7:0]								
0x50	00	Reserved								
0x51	00	Reserved								
0x52	00	Reserved								
0x53	00	Reserved						SCR3[1:0]		
0x54	00	SCR2[1:0]		SCR1[1:0]		Reserved				
0x55	01	Reserved								
0x56	FF	Reserved								
0x57	00	PDB[4]	Reserved							
0x58	00	Reserved		OE[3]	OE[2]	OE[1]	Reserved			
0x59	00	Reserved		PDB[3]	PDB[2]	PDB[1]	Reserved			

Addr	Default Register Hex Value	Bit # 7	6	5	4	3	2	1	0	Description
0x5A	00	REFA[7:0]								**Configuration2** (See definitions from Configuration0 above)
0x5B	00	FBA[10:3]								
0x5C	00	Reserved					FBA[2:0]			
0x5D	00	Reserved	XDIVA	RZA[1:0]		IPA[2:0]			Reserved	
0x5E	00	REFB[7:0]								
0x5F	00	FBB[10:3]								
0x60	00	Reserved								
0x61	00	Reserved								
0x62	00	Reserved								
0x63	00	Reserved								
0x64	00	Reserved								
0x65	40	IPB[5:0]						RZB[1:0]		
0x66	00	Reserved						Reserved	SSENB_B	
0x67	00	Reserved								
0x68	00	Reserved								
0x69	00	Reserved								
0x6A	00	Reserved								
0x6B	00	Reserved								
0x6C	00	REFC[7:0]								
0x6D	00	FBC[10:3]								
0x6E	00	Reserved					FBC[2:0]			
0x6F	00	XDIVC	RZC[1:0]		IPC[2:0]			Reserved		
0x70	00	Reserved								
0x71	00	Reserved								
0x72	00	Reserved								
0x73	00	OD1[7:0]								
0x74	00	OD2[7:0]								
0x75	00	OD3[7:0]								
0x76	00	Reserved								
0x77	00	Reserved								
0x78	00	Reserved								
0x79	00	Reserved						SCR3[1:0]		
0x7A	00	SCR2[1:0]		SCR1[1:0]		Reserved				
0x7B	01	Reserved								
0x7C	FF	Reserved								
0x7D	00	PDB[4]	Reserved							
0x7E	00	Reserved		OE[3]	OE[2]	OE[1]	Reserved			
0x7F	00	Reserved		PDB[3]	PDB[2]	PDB[1]	Reserved			

Marking Diagram (NDG20)



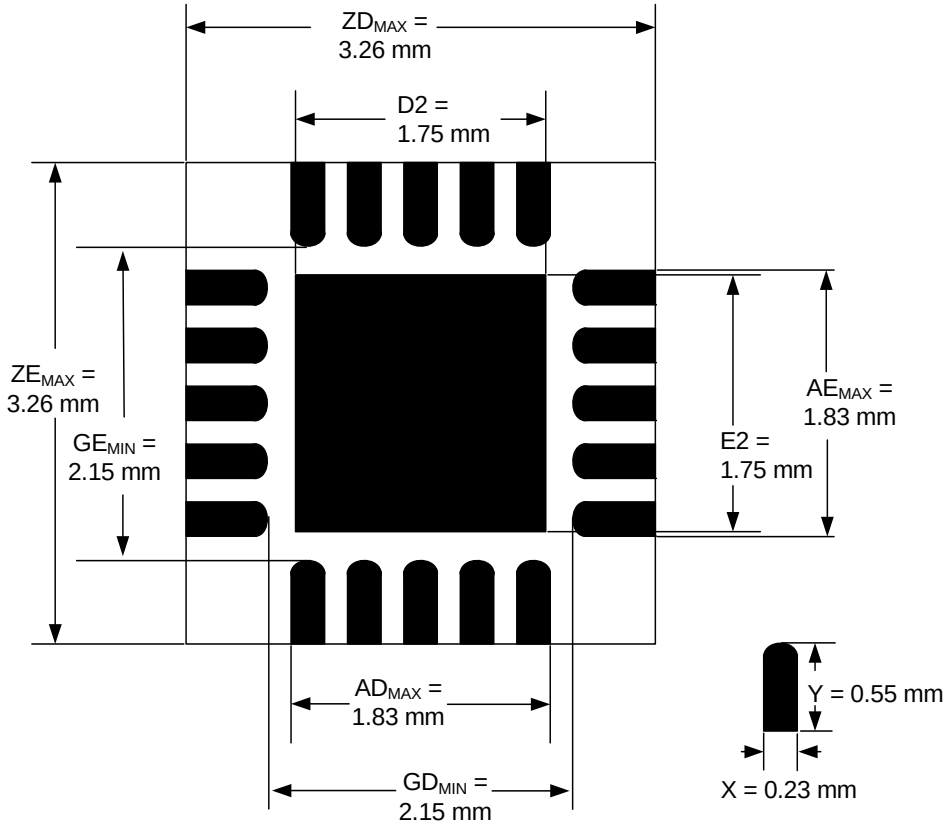
Notes:

1. #### is the lot number.
2. YYWW is the last two digits of the year and week that the part was assembled.
3. “G” designates RoHS compliant package.
4. “I” indicates industrial temperature range.
5. Bottom marking: country of origin if not USA.

Thermal Characteristics 20-pin VFQFPN

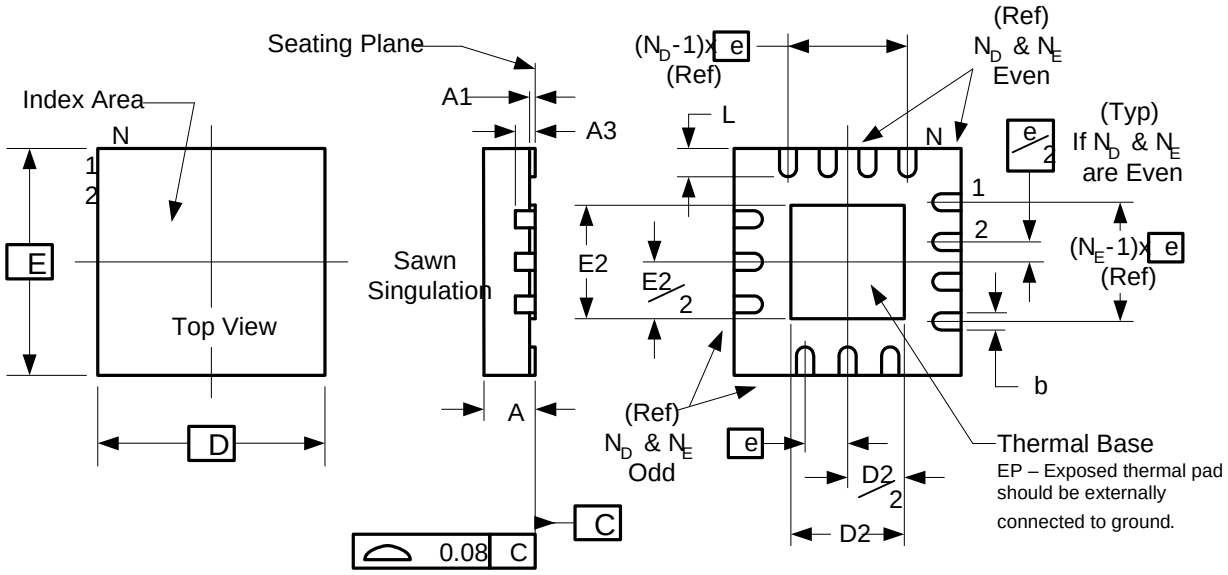
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Thermal Resistance Junction to Ambient	θ_{JA}	Still air		64		°C/W
	θ_{JA}	1 m/s air flow		56.6		°C/W
	θ_{JA}	3 m/s air flow		51.8		°C/W
Thermal Resistance Junction to Case	θ_{JC}			84.3		°C/W

20-pin QFN PCB Land Pattern



Package Outline and Package Dimensions (20-pin QFN)

Package dimensions are kept current with JEDEC Publication No. 95



	Millimeters	
Symbol	**Min**	**Max**
A	0.80	1.00
A1	0	0.05
A3	0.25 Reference	
b	0.15	0.23
e	0.40 BASIC	
N	20	
N_D	5	
N_E	5	
D x E BASIC	3.00 x 3.00	
D2	1.55	1.75
E2	1.55	1.75
L	0.30	0.50

Ordering Information

Part / Order Number	Marking	Shipping Packaging	Package	Temperature
5P49EE515NDGI	See page 20	Tubes	20pin VFQFPN	-40 to +85° C
5P49EE515NDGI8	See page 20	Tape and Reel	20pin VFQFPN	-40 to +85° C

"G" after the two-letter package code are the Pb-Free configuration and are RoHS compliant.

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Revision History

Rev.	Originator	Date	Description of Change
A	R.Willner	06/02/10	Initial Preliminary Datasheet
B	R.Willner	07/26/10	Updated thermal pad and dimensions on package drawing.
C	R.Willner	9/08/10	Power ramp sequenc. Package marking. Thermal pad connected to ground.
D	R. Willner	10/29/10	Typographical changes. Loop filter calculations. Default register bit corrections.
E	R. Willner	01/19/11	Corrected notes for top-side marking.
F	R. Willner	04/13/11	1. Updated SCLK and SDA pin descriptions 2. Updated DC Electrical Char table for 1.8V LVTTL; added VIH and VIL. 3. Updated “Lock Time/PLL Lock Time from shutdown mode” Typ. and Max. specs in AC Timing Electrical Char table.
G	R. Willner	0930/11	Updated Power-up/Power-down Sequence notes.
H	R. Willner	10/17/11	1. Added VDDOx specs to Recommended Operations table 2. Updated Ideal Power-up/Down Sequence diagrams

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