PTAC210802FC

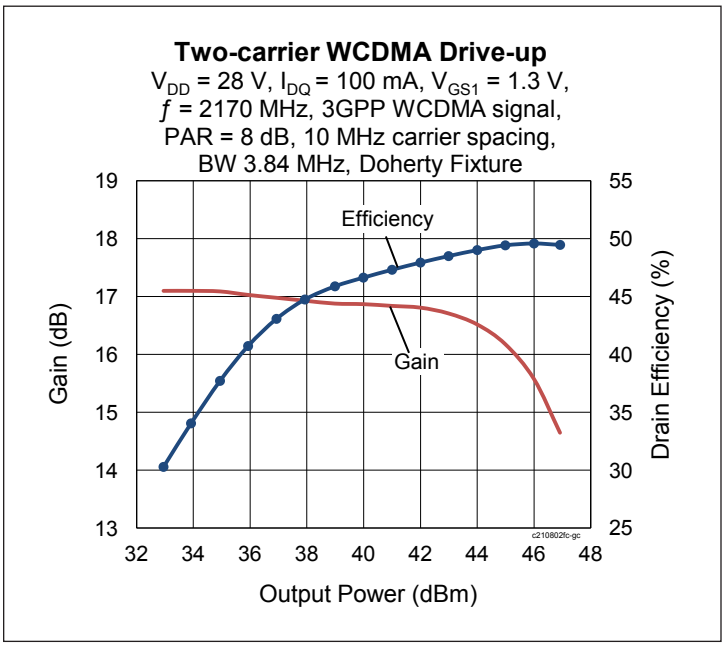
green Product

Thermally-Enhanced High Power RF LDMOS FET
80 W, 28 V, 2110 – 2170 MHz

Description

The PTAC210802FC is an 80-watt LDMOS FET with an asymmetrical design intended for use in multi-standard cellular power amplifier applications in the 2110 to 2170 MHz frequency band. Features include dual-path design, input matching, high gain and thermally-enhanced package with earless flange. Manufactured with Infineon's advanced LDMOS process, this device provides excellent thermal performance and superior reliability.

PTAC210802FC
Package H-37248-4



Features

- Asymmetrical design
  - Main : P1dB = 19 W Typ
  - Peak : P1dB = 60 W Typ
- Broadband internal matching
- Wide video bandwidth
- Typical CW pulsed performance, 2170 MHz, 28 V (Doherty fixture)
  - Output power @ P_{3dB} = 75 W
  - Efficiency = 48%
  - Gain @ P3dB = 14 dB
- Capable of handling 10:1 VSWR @28 V, 80 W (CW) output power
- Integrated ESD protection : Human Body Model, Class 1B (per JESD22-A114)
- Low thermal resistance
- Pb-free and RoHS compliant

RF Characteristics

Two-carrier WCDMA Specifications (tested in Infineon Doherty test fixture)
V_{DD} = 28 V, I_{DQ} = 85 mA, V_{GS1} = 1.3 V, P_{OUT} = 5 W avg, f_1 = 2165 MHz, f_2 = 2175 MHz, 3GPP signal, channel bandwidth = 3.84 MHz, peak/average = 8 dB @ 0.01% CCDF, 10 MHz carrier spacing

Characteristic	Symbol	Min	Typ	Max	Unit
Linear Gain	G_{ps}	15	17	—	dB
Drain Efficiency	η_D	39	43	—	%
Adjacent Channel Power Ratio	ACPR	—	–31	–26	dBc
Output PAR at 0.01% probability on CCDF	OPAR	8	—	—	dB

All published data at T_{CASE} = 25°C unless otherwise indicated

ESD: Electrostatic discharge sensitive device—observe handling precautions!

DC Characteristics (each side)

Characteristic		Conditions	Symbol	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage		V_{GS} = 0 V, I_{DS} = 10 mA	$V_{(BR)DSS}$	65	—	—	V
Drain Leakage Current		V_{DS} = 28 V, V_{GS} = 0 V	I_{DSS}	—	—	1	µA
		V_{DS} = 63 V, V_{GS} = 0 V	I_{DSS}	—	—	10	µA
Gate Leakage Current		V_{GS} = 10 V, I_{DQ} = 0 V	I_{GSS}	—	—	1	V
On-State Resistance	(main)	V_{GS} = 10 V, V_{DS} = 0.1 V	$R_{DS(on)}$	—	0.6	—	Ω
	(peak)	V_{GS} = 10 V, V_{DS} = 0.1 V	$R_{DS(on)}$	—	0.19	—	Ω
Operating Gate Voltage	(main)	V_{DS} = 28 V, I_{DQ} = 85 mA	V_{GS}	2.30	2.65	3.0	V
Operating Gate Voltage	(peak)	V_{DS} = 28 V, I_{DQ} = 360 mA	V_{GS}	2.35	2.70	3.05	V

Maximum Ratings

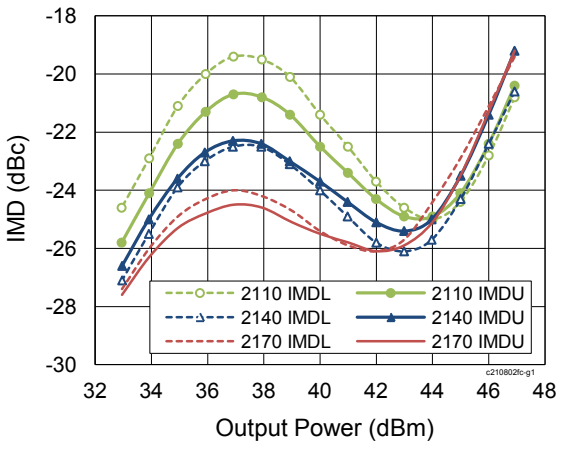
Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	65	V
Gate-Source Voltage	V_{GS}	–6 to +10	V
Operating Voltage	V_{DD}	0 to +32	V
Junction Temperature	T_J	225	°C
Storage Temperature Range	T_{STG}	–65 to +150	°C
Thermal Resistance (main, T_{CASE} = 70°C, 19 W CW)	$R_{\theta JC}$	2.5	°C/W
Thermal Resistance (peak, T_{CASE} = 70°C, 60 W CW)	$R_{\theta JC}$	0.8	°C/W

Ordering Information

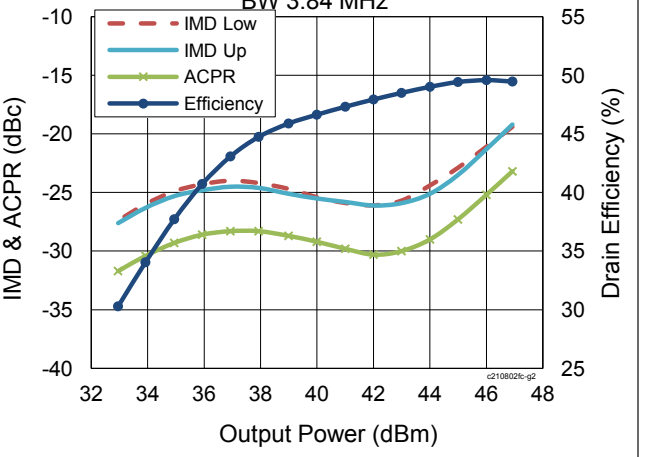
Type and Version	Order Code	Package Description	Shipping
PTAC210802FC V1 R0	PTAC210802FCV1R0XTMA1	H-37248-4, earless flange	Tape & Reel, 50 pcs
PTAC210802FC V1 R250	PTAC210802FCV1R250XTMA1	H-37248-4, earless flange	Tape & Reel, 250 pcs

Typical Performance (data taken in a production Doherty test fixture)

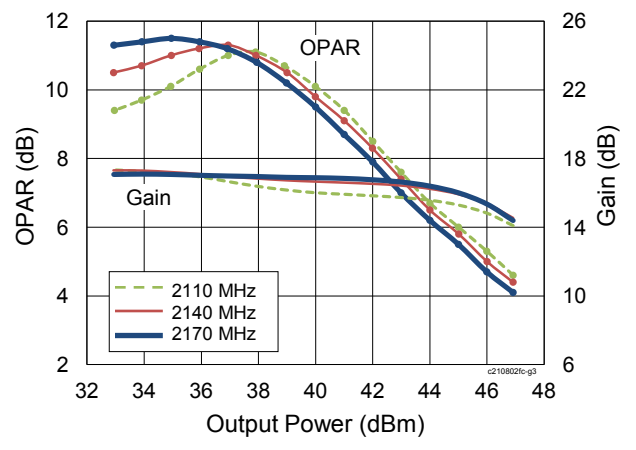
Two-carrier WCDMA Drive-up
V_{DD} = 28 V, I_{DQ} = 100 mA, V_{GS1} = 1.3 V,
3GPP WCDMA signal, PAR = 8 dB,
10 MHz carrier spacing, BW 3.84 MHz



Two-carrier WCDMA Drive-up
V_{DD} = 28 V, I_{DQ} = 100 mA, V_{GS1} = 1.3 V,
f = 2170 MHz, 3GPP WCDMA signal,
PAR = 8 dB, 10 MHz carrier spacing,
BW 3.84 MHz



Single-carrier WCDMA Drive-up
V_{DD} = 28 V, I_{DQ} = 100 mA, V_{GS1} = 1.3 V
3GPP WCDMA signal, PAR = 10 dB,
BW 3.84 MHz



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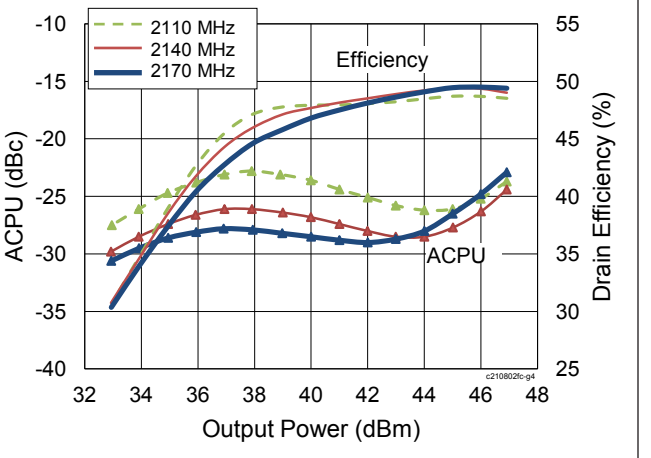
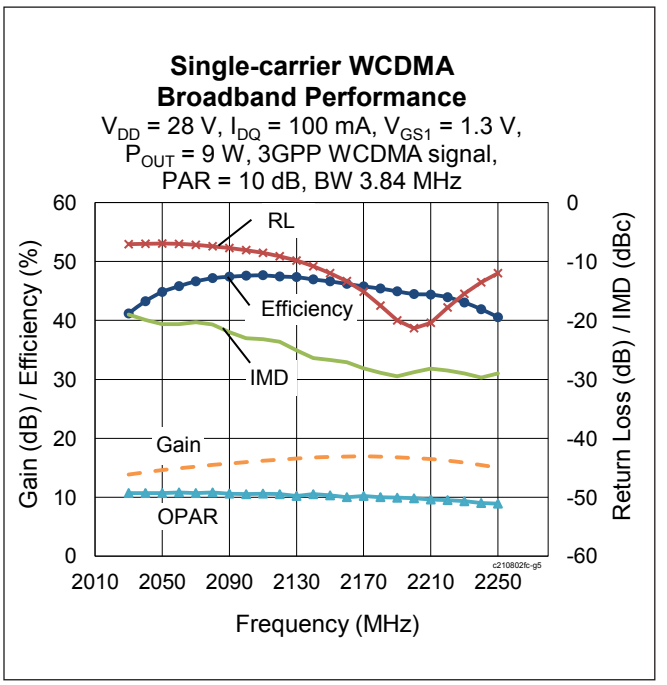
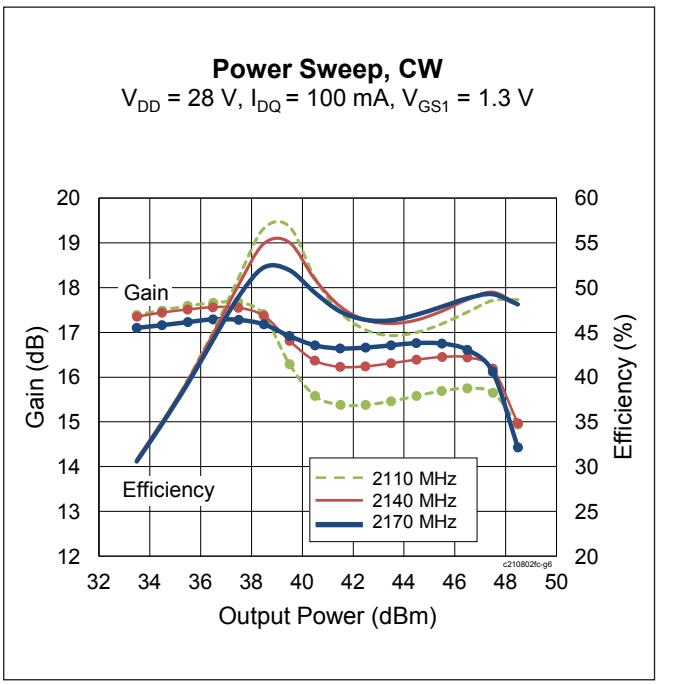
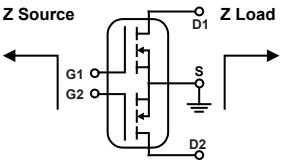


Typical Performance (cont.)





Load Pull Performance



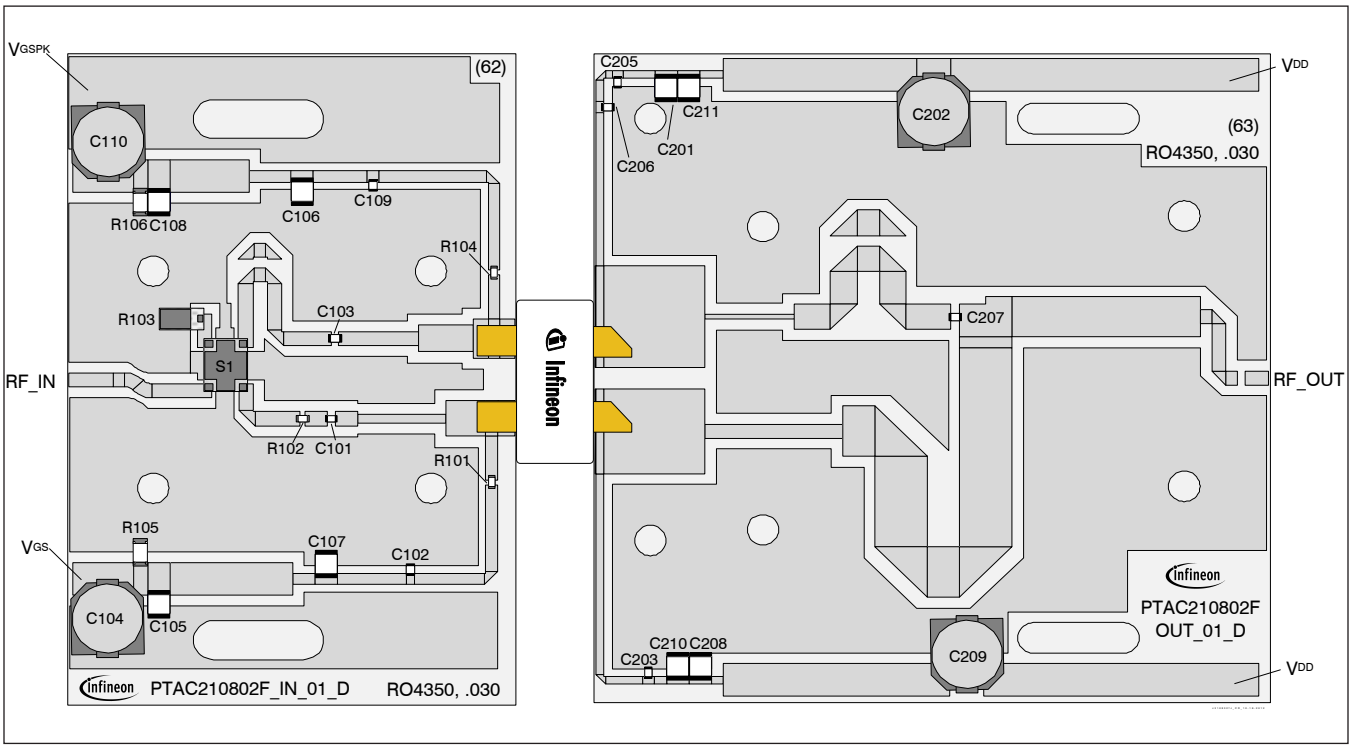
Main Side Load Pull Performance – Pulsed CW signal: 16 µsec, 10% duty cycle; V_{DD} = 28 V, 100 mA

		P_{1dB}									
		Max Output Power					Max PAE				
Freq [MHz]	Zs [Ω]	Zl [Ω]	Gain [dB]	P_{OUT} [dBm]	P_{OUT} [W]	PAE [%]	Zl [Ω]	Gain [dB]	P_{OUT} [dBm]	P_{OUT} [W]	PAE [%]
2110	28.4 – j28.1	15.1 – j11.9	20.8	43.40	22	50	4.6 – j5.2	23.6	41.3	13	68.1
2140	32.4 – j27.7	7.7 – j10	22.0	43.50	22	61	4.15 – j6	23.9	41.3	13	71.9
2170	45.1 – j33.3	10.8 – j10.6	21.6	43.64	23	58	5.2 – j7.2	23.4	42.1	16	68.6

Peak Side Load Pull Performance – Pulsed CW signal: 16 µsec, 10% duty cycle; V_{DD} = 28 V, V_{Gs1} = 1.41 V, Doherty Class C

		P_{3dB}									
		Max Output Power					Max PAE				
Freq [MHz]	Zs [Ω]	Zl [Ω]	Gain [dB]	P_{OUT} [dBm]	P_{OUT} [W]	PAE [%]	Zl [Ω]	Gain [dB]	P_{OUT} [dBm]	P_{OUT} [W]	PAE [%]
2110	14.8 – j14.6	2.4 – j7.4	14.1	49.60	91	62.0	1.6 – j6.0	15.3	48.3	68	72.5
2140	20.6 – j13.6	2.7 – j7.8	14.0	49.50	89	58.8	1.8 – j6.5	15.2	48.7	74	68.5
2170	24.5 – j9.8	2.6 – j8.1	13.9	49.60	91	57.7	2.0 – j6.6	15.3	48.6	72	67.9

Reference Circuit



*Reference circuit assembly diagram (not to scale)**

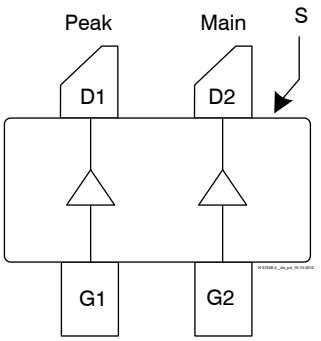
Reference Circuit Assembly	
DUT	PTAC210802FC
Test Fixture Part No.	LTA/PTAC210802FC
PCB	Rogers 4350, 0.762 mm [0.030"] thick, 2 oz. copper, ε_r = 3.66
Find Gerber files for this test fixture on the Infineon Web site at *http://www.infineon.com/rfpower*	

Reference Circuit (cont.)

Components Information

Component	Description	Suggested Supplier	P/N
Input			
C101, C102, C103, C109	Chip capacitor, 24 pF	ATC	ATC800A240JT250XB
C104, C110	Capacitor, 100 µF	Digi-Key	PCE4442TR-ND
C105, C108	Chip capacitor, 0.1 µF	Digi-Key	399-1267-2-ND
C106, C107	Capacitor, 10 µF	Digi-Key	587-1818-2-ND
R101, R102, R104	Resistor, 10 Ω	Digi-Key	P10GCT-ND
R103	Resistor, 50 Ω	Anaren	C16A50Z4
R105, R106	Resistor, 1000 Ω	Digi-Key	P1.0KECT-ND
S1	Hybrid coupler	Anaren	X3C21P1-03S
Output			
C201, C208, C210, C211	Capacitor, 10 µF	Digi-Key	587-1818-2-ND
C202, C209	Capacitor, 220 µF	Digi-Key	PCE4444TR-ND
C203, C204, C205, C206, C207	Chip capacitor, 24 pF	ATC	ATC800A240JT250XB

Pinout Diagram (top view)



Pin	Description
D1	Drain device 1 (Peak)
D2	Drain device 2 (Main)
G1	Gate device 1 (Peak)
G2	Gate device 2 (Main)
S	Source (flange)

Lead connections for PTAC210802FC

Package Outline Specifications

Package H-37248-4

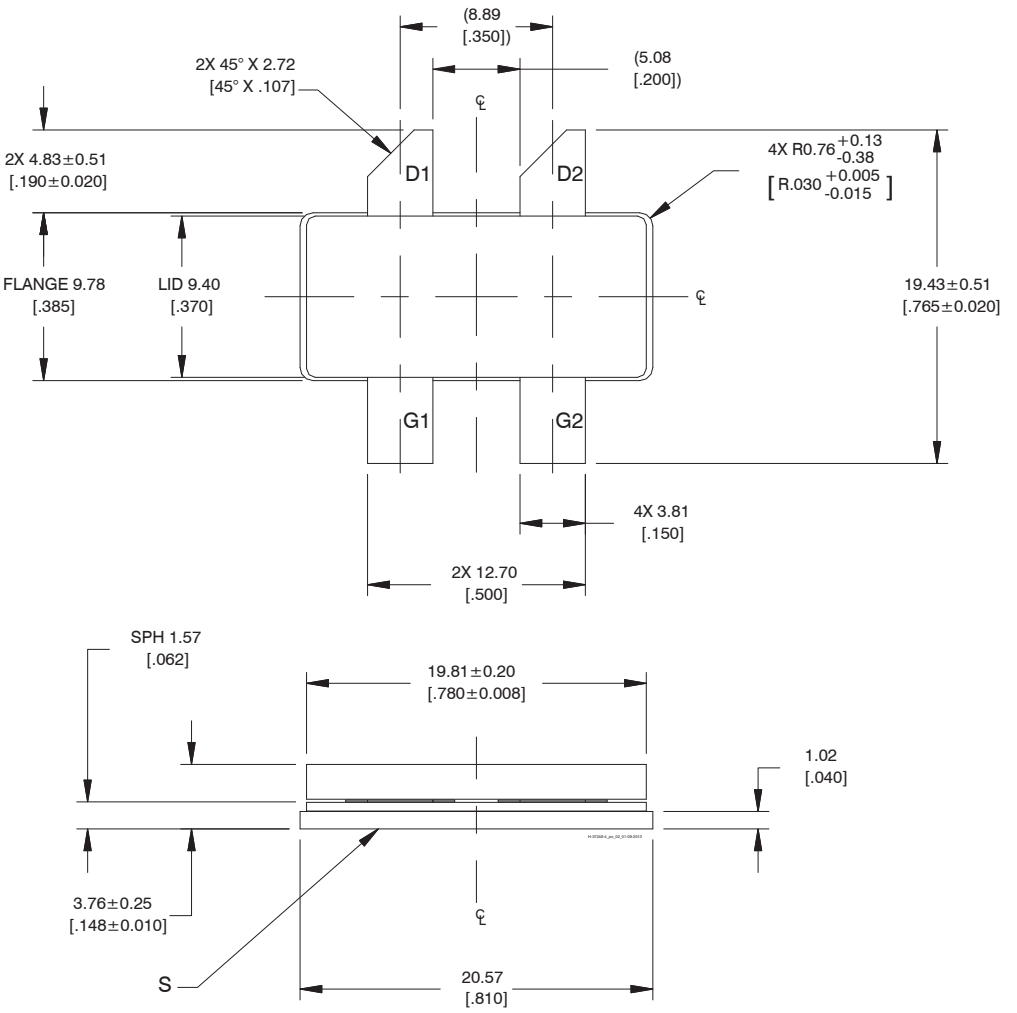


Diagram Notes—unless otherwise specified:

1. Interpret dimensions and tolerances per ASME Y14.5M-1994.
2. Primary dimensions are mm. Alternate dimensions are inches.
3. All tolerances ± 0.127 [.005] unless specified otherwise.
4. Pins: D1, D2 – drains; G1, G2 – gates; S – source.
5. Lead thickness: 0.10 + 0.076/–0.025 mm [0.004+0.003/–0.001 inch].
6. Gold plating thickness: 1.14 ± 0.38 micron [45 ± 15 microinch].

Find the latest and most complete information about products and packaging at the Infineon Internet page http://www.infineon.com/rfpower

Revision History

Revision	Date	Data Sheet Type	Page	Subjects (major changes since last revision)
01	2013-06-11	Advance	All	Data Sheet reflects advance specification for product development
01.1	2012-06-12	Advance	2	Updated power level measured for thermal data
02	2013-10-17	Production	All	Data Sheet reflects released product specification
03	2013-12-17	Production	1 2 7	Added ESD classification, revised two-carrier WCDMA Specifications Added operating voltage in Maximum Ratings table Updated package outline
04	2014-05-14	Production	2	Revised juntion temperature in Maximum Ratings table
05	2014-10-31	Production	1	Revised ESD classification. Corrected IMD to ACPR in RF Characteristics table.
05.1	2015-12-23	Production	2	DC Chracteristic Table
05.2	2016-06-17	Production	2	Updated ordering code to include R0
06	2017-04-07	Production	1	Updated RF Characteristics table to include OPAR

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