40MHz, 32-Channel Serial to Parallel Converter with Push-Pull Outputs

Features

- HVCMOS® technology
- 5.0V logic and 12V supply rail
- Output voltage up to +200V
- Low power level shifting
- Source/sink current minimum 50mA
- 40MHz equivalent data rate
- Latched data outputs
- Forward and reverse shifting options (DIR pin)
- Chip select
- Polarity function

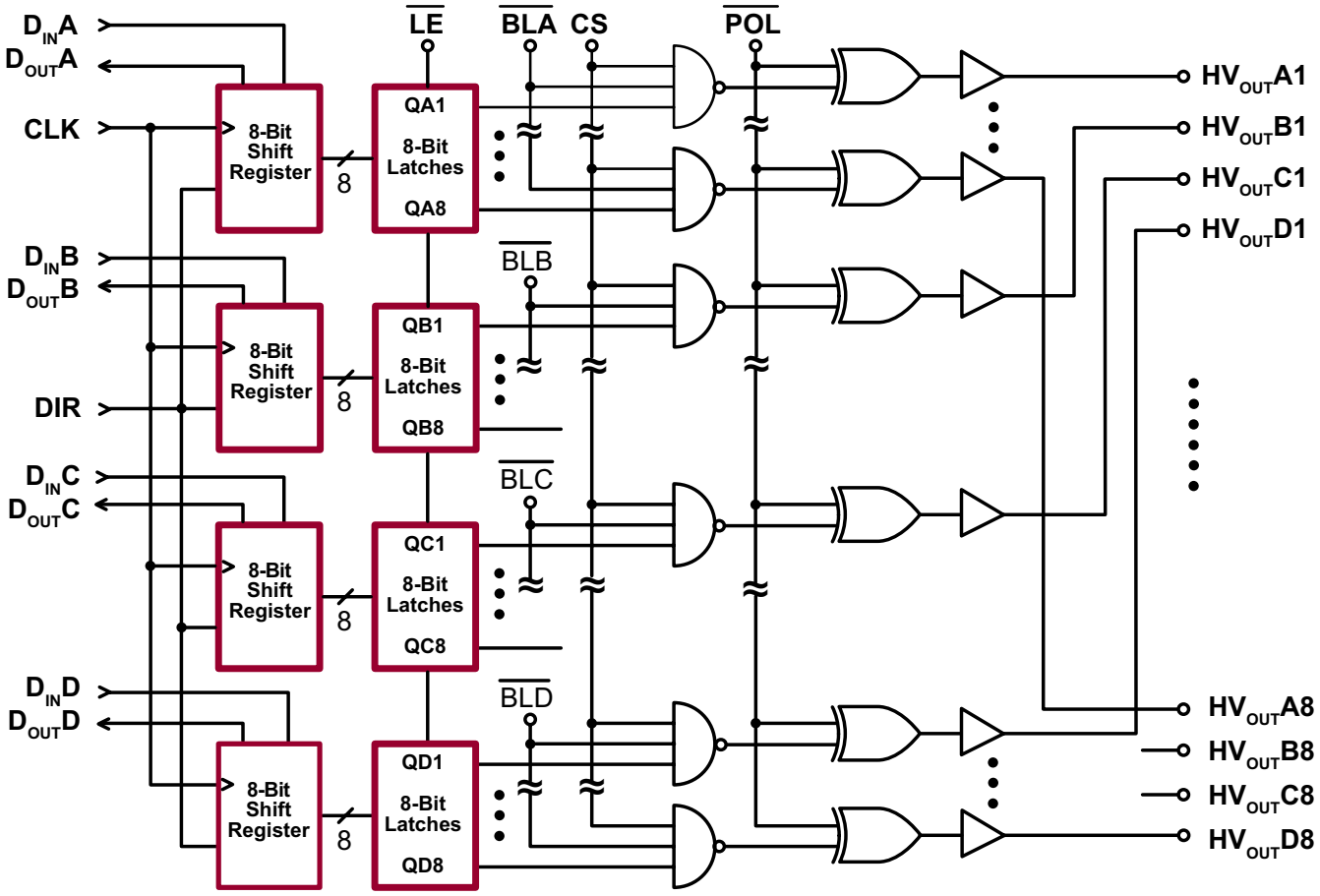
General Description

The HV7620 is a low-voltage serial to high-voltage parallel converter with push-pull outputs. This device has been designed for use as a driver for color AC plasma displays.

The device has 4 parallel 8-bit shift registers permitting data rates four times the speed of one. The data is clocked in simultaneously on all four data inputs with a single clock. Data is shifted in on a low to high transition of the clock. The latches and control logic perform the output enable function.

The DIR pin causes clockwise (CW) shifting of the data when connected to VDD1, and counterclockwise (CCW) shifting when connected to LVGND. Operation of the shift register is not affected by the $\overline{LE}$ (latch enable) input. Transfer of data from the shift registers to the latches occurs when the $\overline{LE}$ input is high. Data is stored in the latches when $\overline{LE}$ is low. The current source on the logic inputs provides active pull up when the input pins are open.

Functional Block Diagram



Ordering Information / Availability

Part Number	Package Option	Packing
HV7620PG-G	64-Lead PQFP (3-sided)	66/tray

-G denotes a lead (Pb)-free / RoHS compliant package

Absolute Maximum Ratings

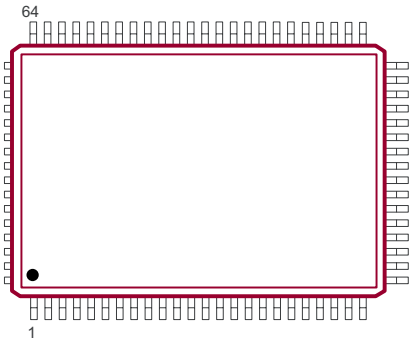
Parameter	Value
Supply voltage, V_{DD1}	-0.5V to +14V
Supply voltage, V_{DD2}	-0.5V to +14V
Supply voltage, V_{PP}	-0.5V to +225V
Logic input levels	-2.0V to V_{DD1} + 2.0V
Continuous total power dissipation[1]	1200mW
Operating temperature range	-40°C to +85°C
Storage temperature range	-65°C to +150°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

Notes:

1. *For operation above 25°C ambient derate linearly to maximum operating temperature at 20mW/°C.*

Pin Configuration



64-Lead PQFP (3-sided)
(top view)

Product Marking

L = Lot Number
YY = Year Sealed
WW = Week Sealed
C = Country of Origin
A = Assembler ID
____ = "Green" Packaging

Package may or may not include the following marks: Si or

64-Lead PQFP (3-sided)

Typical Thermal Resistance

Package	θ_{ja}
64-Lead PQFP	41°C/W

Recommended Operating Conditions

Sym	Parameter		Min	Max	Units
V_{DD1}	Logic supply voltage		4.5	V_{DD2}	V
V_{DD2}	12V supply voltage		10.8	13.2	V
V_{PP}	High voltage supply voltage		50	200	V
V_{IH}	High-level input voltage		V_{DD1} -0.5V	V_{DD1}	V
V_{IL}	Low-level input voltage		0	0.5	V
f_{CLK}	Clock frequency	V_{DD1} = 5.0V	-	10	MHz
		V_{DD1} = 12V	-	5	MHz
T_A	Operating temperature range		-40	+85	°C
I_{OD}	Allowable pulsed current through output diodes[1]		-	500	mA
$I_{GND(VPP)}$	Allowable pulsed V_{PP} or HVGND current[1]		-	16	A
$V_{PP(SLEW)}$	Slew rate of V_{PP}		-	340	V/µs

Notes:

1. *The current pulse width = 500ns, duty cycle = 5%.*

DC Electrical Characteristics

(Over operating supply voltages and temperature, unless otherwise noted, V_{DD1} = 5.0V, V_{DD2} = 12V, V_{PP} = 200V and T_j = 25°C)

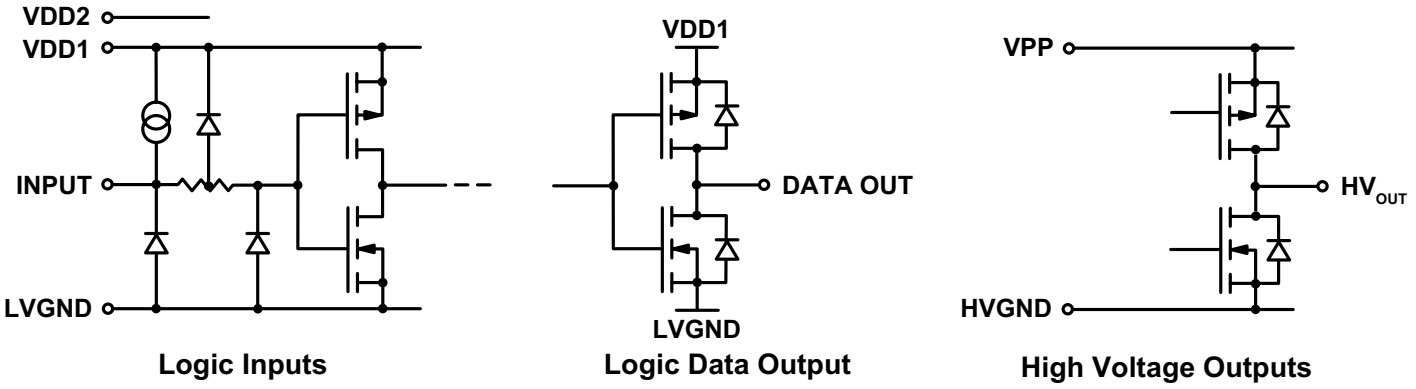
Sym	Parameter		Min	Max	Units	Conditions
I_{DD1}	V_{DD1} supply current		-	5.0	mA	f_{CLK} = 10MHz
I_{DD2}	V_{DD2} supply current		-	20	mA	V_{DD2} = 13.2V, f_{CLK} = 10MHz
I_{PP}	High voltage supply current		-	2.0	mA	All outputs high or low
I_{DD1Q}	Quiescent V_{DD1} supply current		-	100	µA	All input = V_{DD1}
I_{DD2Q}	Quiescent V_{DD2} supply current		-	100	µA	All input = V_{DD1}
V_{OH}	High-level output	HV_{OUT}	185	-	V	I_O = -50mA
		Data OUT	V_{DD} -1	-		I_O = -100µA
V_{OL}	Low-level output	HV_{OUT}	-	20	V	I_O = +50mA
		Data OUT	-	1.0		I_O = +100µA
I_{IH}	High-level logic input current		-	1.0	µA	V_{IN} = V_{DD1}
I_{IL}	Low-level logic input current		-	-10	µA	V_{IN} = 0V
V_{GG}	HVGND to LVGND voltage difference		-1.0	1.0	V	---

AC Electrical Characteristics

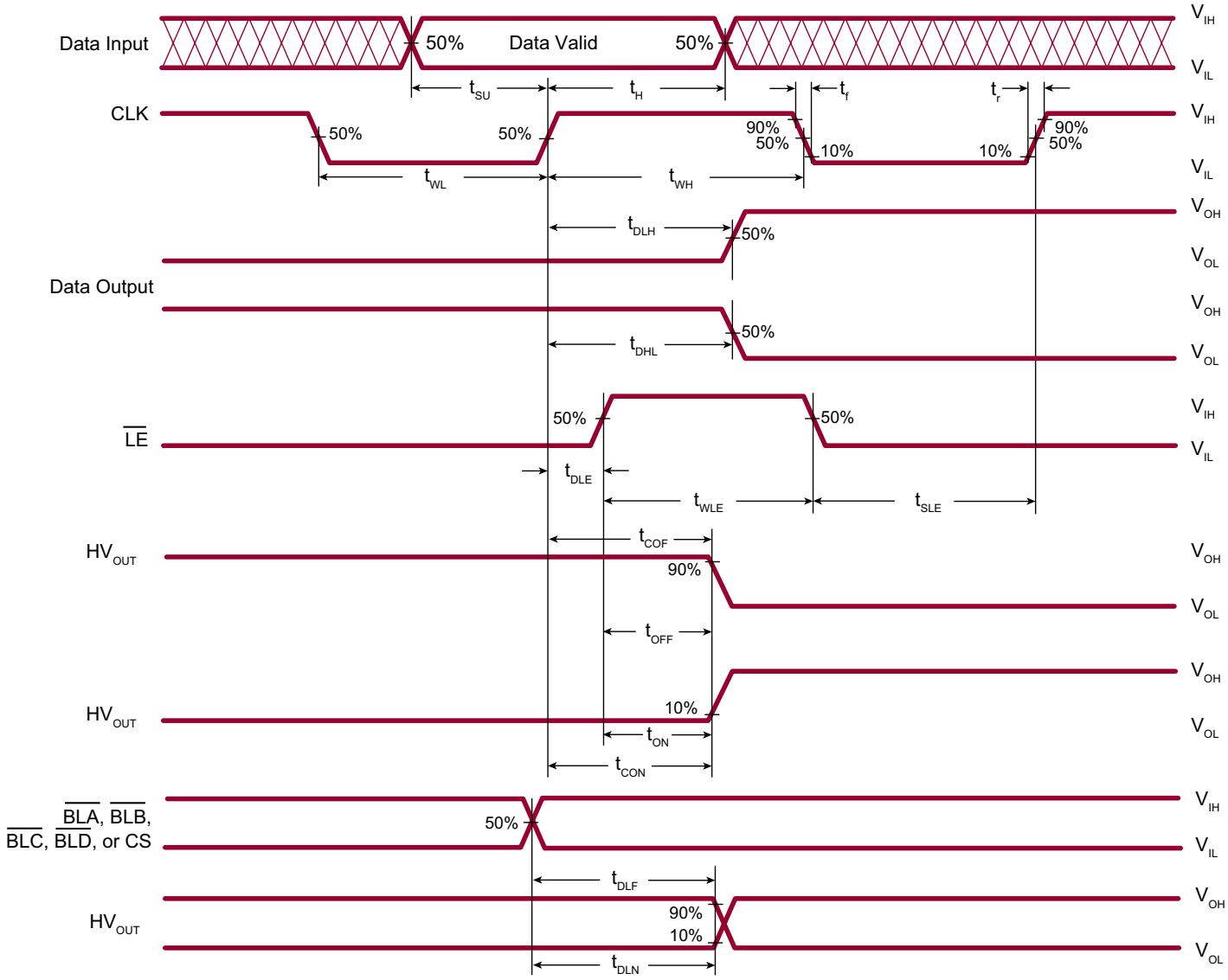
(Logic signal inputs and data inputs have t_r, $t_f \leq$ 5ns. V_{DD1} = 5.0V or 12V, V_{DD2} = 12V, V_{PP} = 200V and T_j = 25°C)

Sym	Parameter		Min	Max	Units	Conditions
f_{CLK}	Clock frequency	V_{DD1} = 5.0V	-	10	MHz	Per register, C_L = 15pF
		V_{DD1} = 12V	-	5.0		
t_{WL}, t_{WH}	Clock width high or low		40	-	ns	---
t_{SU}	Data set-up time before clock rises		20	-	ns	---
t_H	Data hold time after clock rises		20	-	ns	---
t_{ON}, t_{OFF}	Time from latch enable to HV_{OUT}		-	275	ns	C_L = 15pF
t_{WLE}	$\overline{LE}$ pulse width		25	-	ns	---
t_{DLE}	Delay time clock to $\overline{LE}$ low to high		50	-	ns	---
t_{SLE}	$\overline{LE}$ set-up time before clock rises		20	-	ns	---
t_{DLF}, t_{DLN}	$\overline{BL}$ or CS low to high to HV_{OUT}		-	250	ns	---
t_{COF}, t_{CON}	Clock to HV_{OUT}		-	275	ns	---
t_{DLH}	Delay time clock to data low to high	V_{DD1} = 5.0V	-	250	ns	C_L = 15pF
		V_{DD1} = 12V	-	100		
t_{DHL}	Delay time clock to data high to low	V_{DD1} = 5.0V	-	250	ns	C_L = 15pF
		V_{DD1} = 12V	-	100		

Input and Output Equivalent Circuits



Switching Waveforms



Function Table

Function	Inputs													HV_{OUT}			
	$D_{IN}A$	$D_{IN}B$	$D_{IN}C$	$D_{IN}D$	CLK	$\overline{LE}$	DIR	$\overline{BLA}$	$\overline{BLB}$	$\overline{BLC}$	$\overline{BLD}$	CS	$\overline{POL}$	A	B	C	D
All O/P High	X	X	X	X	X	X	X	X	X	X	X	L	L	H	H	H	H
All O/P Low	X	X	X	X	X	X	X	X	X	X	X	L	H	L	L	L	L
"A"† Outputs Low	X	X	X	X	X	X	X	L	X	X	X	X	H	L	*	*	*
Normal Polarity	X	X	X	X	X	X	X	H	H	H	H	H	H	No Inversion			
Outputs Inverted	X	X	X	X	X	X	X	H	H	H	H	H	L	Inversion			
Transparent Mode	H	L	L	L	↑	H	X	H	H	H	H	H	H	H	L	L	L
Data Stored	X	X	X	X	X	L	X	H	H	H	H	H	H	Stored data			
Shift CW[A]	X	X	X	X	↑	H	H	H	H	H	H	H	X	$A_N \rightarrow A_{N+1}$	$B_N \rightarrow B_{N+1}$	$C_N \rightarrow C_{N+1}$	$D_N \rightarrow D_{N+1}$
Shift CCW[B]	X	X	X	X	↑	H	L	H	H	H	H	H	X	$A_N \rightarrow A_{N-1}$	$B_N \rightarrow B_{N-1}$	$C_N \rightarrow C_{N-1}$	$D_N \rightarrow D_{N-1}$

Notes:

H = High level, L = Low level, X = Irrelevant, ↑ = Low to high transition.

** = Dependent on previous stage's state before the last CLK ↑ for last $\overline{LE}$ high.*

† = $\overline{BLB}$, $\overline{BLC}$ and $\overline{BLD}$ will have similar effect on their respective output.

Power-up sequence:

1. *GND (HV, LV)*
2. *V_{DD1}*
3. *V_{DD2}*
4. *V_{PP}*
5. *Logic Input Signals*

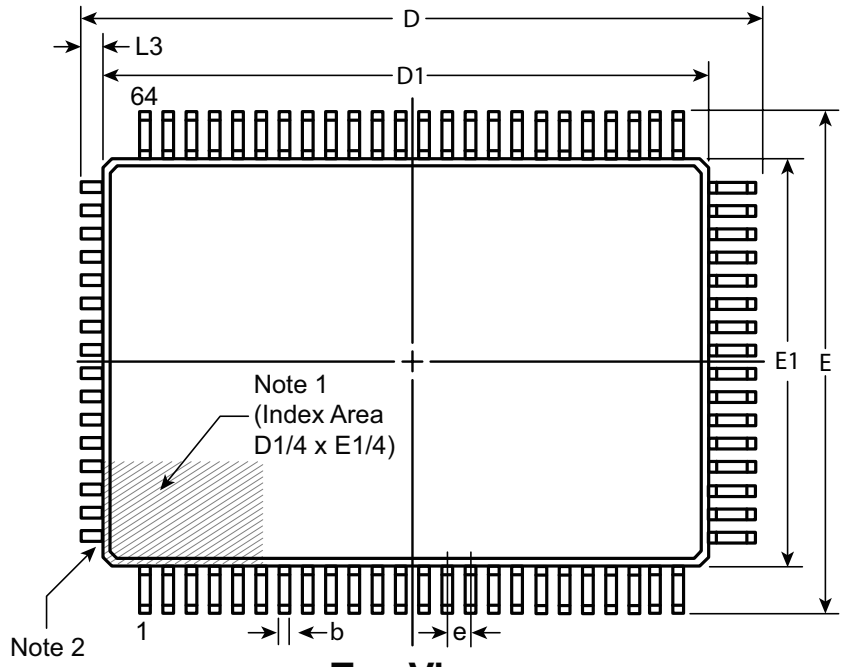
To power down reverse the sequence above.

Pin Function

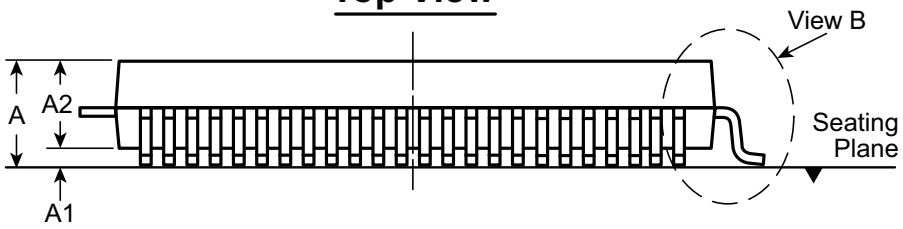
Pin #	Function
1	HVGND
2	VPP
3	$HV_{OUT}D8$
4	$HV_{OUT}C8$
5	$HV_{OUT}B8$
6	$HV_{OUT}A8$
7	$HV_{OUT}D7$
8	$HV_{OUT}C7$
9	$HV_{OUT}B7$
10	$HV_{OUT}A7$
11	$HV_{OUT}D6$
12	$HV_{OUT}C6$
13	$HV_{OUT}B6$
14	$HV_{OUT}A6$
15	$HV_{OUT}D5$
16	$HV_{OUT}C5$
17	$HV_{OUT}B5$
18	$HV_{OUT}A5$
19	VPP
20	HVGND
21	HVGND
22	VDD2
23	$\overline{BLC}$
24	$\overline{BLD}$
25	$\overline{LE}$
26	$D_{OUT}D$
27	$D_{IN}D$
28	$D_{IN}C$
29	$D_{OUT}C$
30	$\overline{POL}$
31	LVGND
32	DIR
33	CS
34	$D_{OUT}B$
35	$D_{IN}B$
36	$D_{IN}A$
37	$D_{OUT}A$
38	CLK
39	$\overline{BLA}$
40	$\overline{BLB}$
41	VDD1
42	LVGND
43	N/C
44	HVGND
45	HVGND
46	VPP
47	$HV_{OUT}D4$
48	$HV_{OUT}C4$
49	$HV_{OUT}B4$
50	$HV_{OUT}A4$
51	$HV_{OUT}D3$
52	$HV_{OUT}C3$
53	$HV_{OUT}B3$
54	$HV_{OUT}A3$
55	$HV_{OUT}D2$
56	$HV_{OUT}C2$
57	$HV_{OUT}B2$
58	$HV_{OUT}A2$
59	$HV_{OUT}D1$
60	$HV_{OUT}C1$
61	$HV_{OUT}B1$
62	$HV_{OUT}A1$
63	VPP
64	HVGND

64-Lead PQFP (3-Sided) Package Outline (PG)

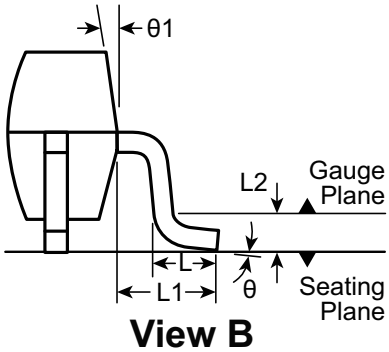
20.00x14.00mm body, 3.40mm height (max), 0.80mm pitch, 3.90mm footprint



Top View



Side View



View B

Note:

1. *A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*
2. *The leads on this side are trimmed.*

Symbol		A	A1	A2	b	D	D1	E	E1	e	L	L1	L2	L3	θ	θ1
Dimension (mm)	MIN	2.80	0.25	2.55	0.30	22.25	19.80	17.65	13.80	0.80 BSC	0.73	1.95 REF	0.25 BSC	0.55 REF	0°	5°
	NOM	-	-	2.80	-	22.50	20.00	17.90	14.00		0.88				3.5°	-
	MAX	3.40	0.50	3.05	0.45	22.75	20.20	18.15	14.20		1.03				7°	16°

Drawings not to scale.
Supertex Doc. #: *DSPD-64PQFPPG, Version A080812.*

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to http://www.supertex.com/packaging.html.)

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