◇Structure Silicon Monolithic integrated circuit
◇Product name Audio interface LSI
◇Type BU7620GUW
◇Applications Record and Playback devices such as DSC, Voice Recorder, etc
◇Functions
- Monaural 16 bit ΔΣCODEC
- Monaural microphone amplifier with ALC function
- Monaural line amplifier
- BTL output speaker amplifier 400mW@8Ω)
- 48-step electronic volume with ALC function
- PLL built-in (Reference clock: 12MHz、24MHz、27MHz、16fs、32fs、64fs)
  (Sampling rate: 8kHz ～ 48kHz)
  (Master clock output)
- 3-wire serial interface (power on reset function)
- Audio IF format, 2's compliment
  <ADC> 16bit word lengths Left justified, I²S DSP
  <DAC> 16bit word lengths Left, Right justified, I²S DSP

◇Absolute maximum ratings (Ta=25℃)

Parameter	Symbol	Limits	Unit	Comment
Supply voltage	VDD	−0.3～4.5	V	AVDD、DVDD、SPVDD
Input voltage	VIN	−0.3～supply voltage +0.3	V	keep each limits upon
Storage temperature range	TSTG	−50～125	℃	
Operating temperature range	TOPE	−20～85	℃	
Power dissipation *1	PD	520	mW	

* 1 : In the case of use at Ta=25℃ or more, 5.2mW should be reduced per 1℃.
(t=1.6mm, 114.3mm x 76.2mm, board base on SEMI, 4-layer board)
Radiation resistance design is not arranged.

◇ Operating conditions (Ta=25℃)

Parameter	Symbol	Limits	Unit	Comment
Supply voltage	VDD	2.7～3.6	V	AVDD、DVDD、SPVDD

(note) AVDD、DVDD、SPVDD、VVDD are not needed to be same voltage.
(note) Please do not set SPVDD lower than AVDD−0.3V.

◇Electrical characteristics
(Unless specified, Ta=25℃、AVDD=SPVDD=DVDD= 3.3V、AVSS=SPVSS=DVSS= 0V、B.W.=22Hz～22kHz、fs=48kHz、fin=1kHz)

Parameter	Symbol	Limits			Unit	Condition
		MIN.	TYP.	MAX.		
< Current consumption > #MASTER=0 MCLK=24MHz						
Power-down mode	IDDS	−	0.02	0.1	mA	#PWAP=MDPLL=0
Rec mode/PLL mode	IDDR	−	7.0	14.0	mA	#MDREC=MDPLL=1
Play mode/PLL mode	IDDP	−	8.0	16.0	mA	#MDPB=MDSP=MDPLL=1
<MREG>						
output voltage	VOREG	0.75AVDD −0.2	0.75AVDD	0.75AVDD +0.2	V	2.2kΩ load
< Logic interface >						
L input voltage	VIL	DVSS	—	0.3DVDD	V	
H input voltage	VIH	0.7DVDD	—	DVDD	V	
L input voltage	IIL	—	—	10	μA	
H input voltage	IIH	—	—	10	μA	
L output voltage	VOL	0	—	0.5	V	IOL=−1mA
H output voltage	VOH	DVDD−0.5	—	DVDD	V	IOL=1mA
<REC path (MICIN→ADOUT)> #ALC1=OFF, MGAIN=48dB						
Input impedance	ZIN	65	95	125	kΩ	
Input level	VIN	−52.0	−50.0	−48.0	dBV	DOUT=0dBFS
Distortion	THD+N	43	58	−	dB	DOUT=−6dBFS@1kHz
SNR	SNR	60	67	−	dB	B.W.=JIS-A
ALC1 output level	DOALC	−	−7.3	−	dBFS	ALC1=ON

Status of this document
The Japanese version of this document is the formal specification. A customer may use this translation version only for a reference to help reading the formal version. If there are any differences in translation version of this document, formal version takes priority.

◇Electrical characteristics

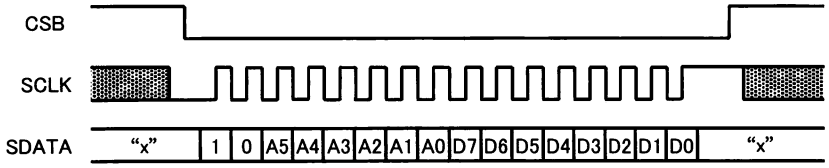
(Unless specified, Ta=25℃、AVDD=SPVDD=DVDD= 3.3V、AVSS=SPVSS=DVSS= 0V、B.W.=22Hz～22kHz、fs=48kHz、fin=1kHz)

< PB path1 (DAIN→LINEOUT)> #LGAIN=+5dB						
Output level	VO	-5.5	-4.0	-2.5	dBV	DIN=-6dBFS
Distortion	THD+N	59	79	-	dB	DIN=-6dBFS@1kHz
SNR	SNR	80	88	-	dB	B.W.=JIS-A
< PB path2 (DAIN→EVROUT→SPIN→SPOUT BTL 出力)> #ALC2=OFF, EVR=-6dB, RL=8Ω						
Output level	VO	1.0	3.0	5.0	dBV	DIN=0dBFS
Distortion	THD+N	47	62	-	dB	DIN=0dBFS@1kHz
SNR	SNR	76	83	-	dB	B.W.=JIS-A
ALC2 output level	VOALC	1.0	3.0	5.0	dBV	ALC2=ON, EVR=8dB

(note) Input level of REC and Output level of PB is relative to AVDD.

◇Serial interface

Control commands are entered on the CSB, SCLK, and SDATA pins, using 3 line 16 bit serial input (MSB first).
The input cycle is started on the CSB falling edge, and each bit of data is read in on the SCLK rising edge.
The data is loaded to register on the CSB rising edge.



Register Address : A5 - A0
Control Data : D7 - D0

◇Register map

Address	Register	D7	D6	D5	D4	D3	D2	D1	D0
00H	Power control	0	PWSV	PWAP	PWMRG	0	0	0	PWDRG
01H	Power control	0	COMENB	0	0	MDSP	MDPB	MDREC	MDPLL
03H	Gain control	0	VMRG	ADA	0	0	LGAIN	MGAIN1	MGAIN0
04H	Gain control	0	0	0	0	MUSP	0	MULO	MUDVL
05H	Clock control	FMCK1	FMCK0	FBCK1	FBCK0	DIFGS	DIF2	DIF1	DIF0
06H	Clock control	0	FRCK2	FRCK1	FRCK0	SFS1	SFS0	DIV1	DIV0
07H	Clock control	MASTER	BFPD	0	DLEN	0	MCKO	0	0
08H	ALC control	0	MDALC1	MDEVR1	MDEVR0	0	0	0	MDDVL
09H	ALC control	ATMC1	ATMC0	RCMC1	RCMC0	ATSP1	ATSP0	RCSP1	RCSP0
0AH	ALC control	RC2MC1	RC2MC0	CVRG1	CVRG0	RCLM	0	0	0
0BH	Time control	RINI2	RINI1	RINI0	PINI1	PINI0	0	DVLT	EVRT
0CH	Volume control	0	MLIM6	MLIM5	MLIM4	MLIM3	MLIM2	MLIM1	MLIM0
0DH	Filter control	0	0	0	0	HPFR3	HPFR2	HPFR1	HPFR0
0EH	Volume control	DVOL7	DVOL6	DVOL5	DVOL4	DVOL3	DVOL2	DVOL1	DVOL0
0FH	Volume control	0	0	EVR5	EVR4	EVR3	EVR2	EVR1	EVR0
10H	Volume control	0	0	SPVOL1	SPVOL0	0	0	0	0
17H	Filter control	DFMRP	OLDFM	0	DFMEN4	DFMEN3	DFMEN2	DFMEN1	DFMEN0
18H	Filter control	DF0M1	DF0M0	DF0A13	DF0A12	DF0A11	DF0A10	DF0A9	DF0A8
19H	Filter control	DF0A7	DF0A6	DF0A5	DF0A4	DF0A3	DF0A2	DF0A1	DF0A0
1AH	Filter control	0	0	DF0B13	DF0B12	DF0B11	DF0B10	DF0B9	DF0B8
1BH	Filter control	DF0B7	DF0B6	DF0B5	DF0B4	DF0B3	DF0B2	DF0B1	DF0B0
1CH	Filter control	DF1M1	DF1M0	DF1A13	DF1A12	DF1A11	DF1A10	DF1A9	DF1A8
1DH	Filter control	DF1A7	DF1A6	DF1A5	DF1A4	DF1A3	DF1A2	DF1A1	DF1A0
1EH	Filter control	0	0	DF1B13	DF1B12	DF1B11	DF1B10	DF1B9	DF1B8
1FH	Filter control	DF1B7	DF1B6	DF1B5	DF1B4	DF1B3	DF1B2	DF1B1	DF1B0
20H	Filter control	DF2M1	DF2M0	DF2A13	DF2A12	DF2A11	DF2A10	DF2A9	DF2A8
21H	Filter control	DF2A7	DF2A6	DF2A5	DF2A4	DF2A3	DF2A2	DF2A1	DF2A0
22H	Filter control	0	0	DF2B13	DF2B12	DF2B11	DF2B10	DF2B9	DF2B8
23H	Filter control	DF2B7	DF2B6	DF2B5	DF2B4	DF2B3	DF2B2	DF2B1	DF2B0
24H	Filter control	DF3M1	DF3M0	DF3A13	DF3A12	DF3A11	DF3A10	DF3A9	DF3A8
25H	Filter control	DF3A7	DF3A6	DF3A5	DF3A4	DF3A3	DF3A2	DF3A1	DF3A0
26H	Filter control	0	0	DF3B13	DF3B12	DF3B11	DF3B10	DF3B9	DF3B8
27H	Filter control	DF3B7	DF3B6	DF3B5	DF3B4	DF3B3	DF3B2	DF3B1	DF3B0
28H	Filter control	DF4M1	DF4M0	DF4A13	DF4A12	DF4A11	DF4A10	DF4A9	DF4A8
29H	Filter control	DF4A7	DF4A6	DF4A5	DF4A4	DF4A3	DF4A2	DF4A1	DF4A0
2AH	Filter control	0	0	DF4B13	DF4B12	DF4B11	DF4B10	DF4B9	DF4B8
2BH	Filter control	DF4B7	DF4B6	DF4B5	DF4B4	DF4B3	DF4B2	DF4B1	DF4B0

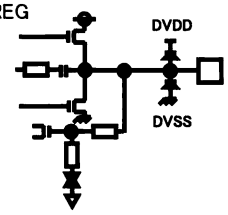
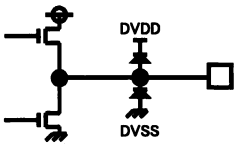
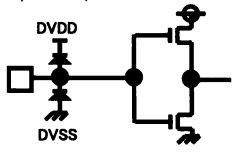
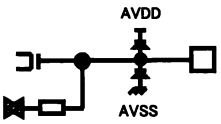
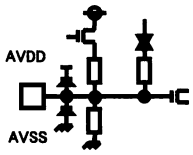
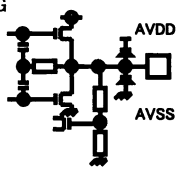
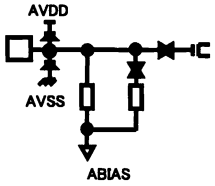
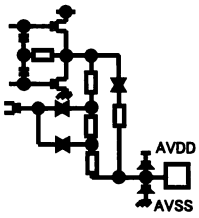
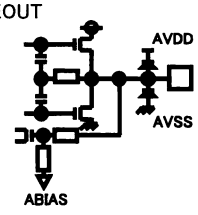
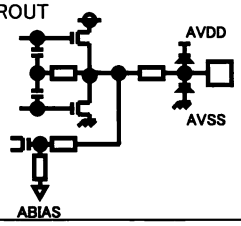
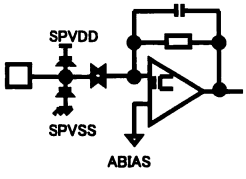
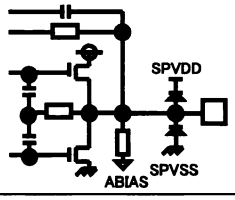
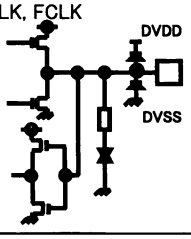
(note) Do not write to the address except for the above.

◇Pin Functional Descriptions

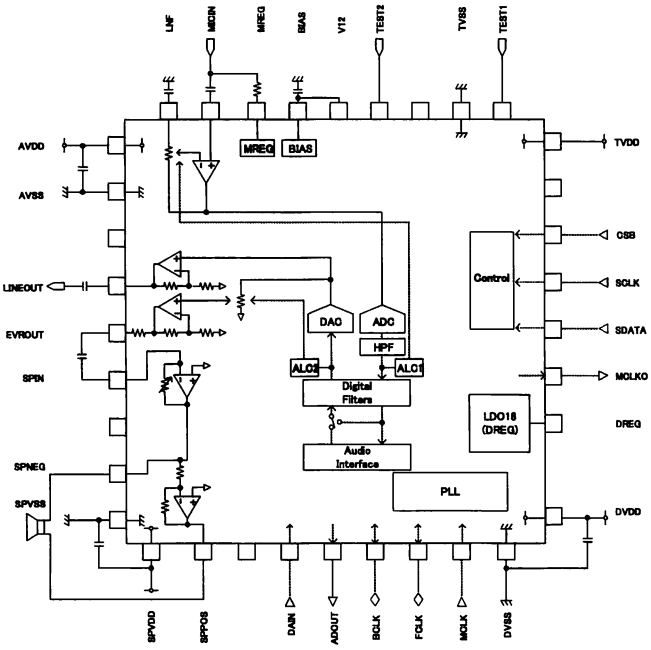
No		Pin name	Function
1	A1	DVDD	Digital power supply
2	–	N.C.	–
3	C3	DREG	LDO18 output (1.8V)
4	C1	MCLKO	CODEC master clock output
5	C2	SDATA	3-wire serial data input
6	D1	SCLK	3-wire serial clock input
7	D2	CSB	3-wire serial chip select input
8	E1	TVDD	Power supply for test circuit(=DVDD)
9	E2	N.C.	–
10	F1	TEST1	Test terminal1(OPEN)
11	F2	TVSS	Ground for test circuit(short to DVSS)
12	D3	N.C.	–
13	F3	TEST2	Test terminal2(OPEN)
14	E3	V12	MIC power supply standard voltage
15	F4	BIAS	Bias (1/2AVDD)
16	E4	MREG	MIC power supply
17	F5	MICIN	MIC input
18	E5	LNF	MIC NF input

No		Pin name	Function
19	F6	AVDD	Analog power supply
20	E6	AVSS	Analog ground
21	D4	N.C	–
22	D6	LINEOUT	LINE output
23	D5	EVROUT	EVR output
24	C6	SPIN	SP input
25	C5	N.C.	–
26	B6	SPNEG	SP negative output
27	B5	SPVSS	SP ground
28	A6	SPVDD	SP power supply
29	A5	SPPOS	SP positive output
30	C4	N.C.	–
31	A4	DAIN	CODEC DA serial data input
32	B4	ADOUT	CODEC AD serial data output
33	A3	BCLK	CODEC bit clock in/output
34	B3	FCLK	CODEC frame clock in/output
35	A2	MCLK	CODEC master clock input
36	B2	DVSS	Digital ground

◇Pin Peripheral Circuits

PIN		Equivalent circuit	PIN		Equivalent circuit	PIN		Equivalent circuit
3	C3	DREG 	4 32	C1 B4	MCLKO , ADOUT 	5 6 7 31 35	C2 D1 D2 A4 A2	SDATA, SCLK, CSB DAIN, MCLK, 
PIN		Equivalent circuit	PIN		Equivalent circuit	PIN		Equivalent circuit
14	E3	V12 	15	F4	BIAS 	16	E4	MREG 
PIN		Equivalent circuit	PIN		Equivalent circuit	PIN		Equivalent circuit
17	F5	MICIN 	18	E5	LNF 	22	D6	LINEOUT 
PIN		Equivalent circuit	PIN		Equivalent circuit	PIN		Equivalent circuit
23	D5	EVROUT 	24	C6	SPIN 	26 29	B6 A5	SPNEG, SPPOS 
PIN		Equivalent circuit						
33 34	A3 B3	BCLK, FCLK 						

◇Block diagram・External dimensions



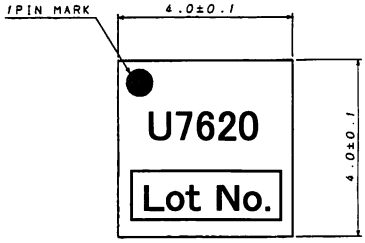
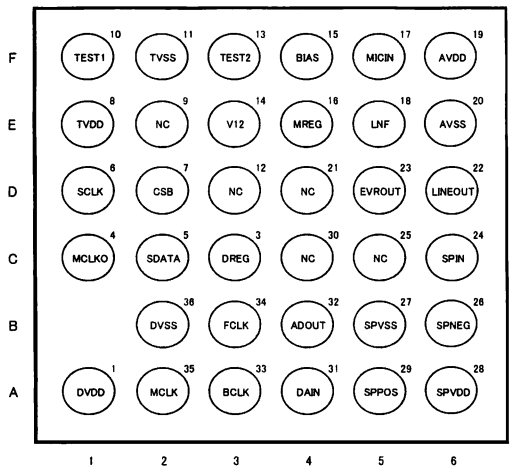


Figure 1 Block diagram



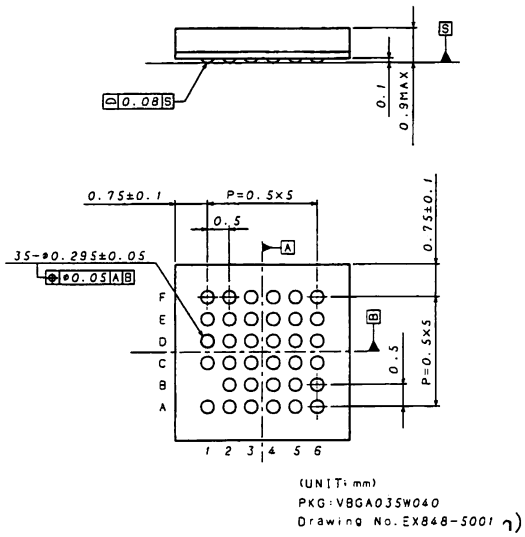


Figure 2 A terminal layout plan (Bottom view)

◇Caution

(1) About absolute maximum rating

When the absolute maximum rating such as the applied voltage and the ranges of the operating temperature is exceeded, LSI might be destroyed. Please apply neither voltage nor the temperature that exceeds the absolute maximum rating. Please execute physical measures for safety such as fuse when it is thought to exceed the absolute maximum rating, and examine it so that the condition to exceed the absolute maximum rating is not applied to LSI.

(2) About GND Voltage

In any state of operation must be the lowest voltage about the voltage of the terminal GND. Please actually confirm the voltage of each terminal is not a voltage that is lower than the terminal GND including excessive phenomenon.

(3) About design of overheating malfunction preventive circuit

Please design overheating malfunction preventive circuit with an enough margin in consideration of a permissible loss in the state of using actually.

(4) About the short between terminals and the mounting by mistake

Please note the direction and the gap of position of LSI enough about LSI when you mount on the substrate. LSI might be destroyed when mounting by mistake and energizing. Moreover, LSI might be destroyed when short-circuited by entering of the foreign substances between the terminal and GND, between terminals, between the terminal and the power supply of LSI.

(5) About operation in strong electromagnetic field

Use in strong electromagnetic field has the possibility of malfunctioning and evaluate it enough, please.

(6) Please note not to be beyond the package permissible range, When SPVDD is set.

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